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FINAL REPORT
entitled
**TRENDS AND TECHNIQUES FOR
SPACE BASE ELECTRONICS**

June, 1979

(NASA-CR-161270) TRENDS AND TECHNIQUES FOR
SPACE BASE ELECTRONICS Final Report, 10
Mar. 1978 - 9 Mar. 1979

(Mississippi State
Univ., Mississippi State.) 245 p

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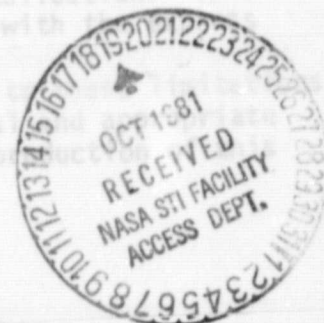
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TRENDS AND TECHNIQUES FOR SPACE BASE ELECTRONICS

Final Report
June 1979

SUMMARY

During the reporting period of this contract, four activities were in progress:

- 1) the completion of the 2-D diffusion studies in SOS,
- 2) the set-up of a sputtering system, furnaces, and photolithography related equipment at MSU,
- 3) experiments on double layer metal, and
- 4) the investigation of 2-D modeling of MOSFETs.

Using the 2-D diffusion program developed in the previous contract period, simulations of various phosphorus and boron diffusions in SOS have been completed.

The MSU I. C. Laboratory has in place the furnaces, the photolithography facilities and metallization system to reproduce the NASA/Huntsville double layer metal process - the only missing equipment being the SiO_2 vapox reactor.

The double layer metal activity initially emphasized wet chemistry techniques. By incorporating the following techniques:

(1) ultrasonic etching of the vias, (2) premetal clean using a modified buffered HF, (3) phosphorus doped vapox, and (4) extended sintering, yields of 98% were obtained using the standard test pattern.

A two dimensional modeling program has been written for the simulation of short channel MOSFETs with nonuniform substrate doping. A key simplifying assumption used is that the majority carriers can be represented by a sheet charge at the silicon dioxide-silicon interface. The program is not complete. In solving current continuity equation, the program does not converge. However, solving the 2-dimensional Poisson equation for the potential distribution has been achieved. The status of other 2-D MOSFET simulation programs are summarized.

I. REDISTRIBUTION DIFFUSIONS FOR ION-IMPLANTED PREDEPOSITS OF BORON AND PHOSPHORUS IN SOS FILMS

The objective of this work was to produce curves describing the variation with diffusion time and temperature of the junction depth, sheet resistance and integrated impurity dose. This data has been generated for boron and phosphorus redistributed in nitrogen, dry oxygen and steam ambients for <111> oriented SOS films. The following section presents discussions of the implantation and redistribution model, further program develop, the computational procedure and of the computed results.

A. The Redistribution Model

There are three aspects of the redistribution model which are considered: (a) the implanted profile, (b) the oxidation model, and (c) the diffusivity model.

a.) The implanted profile, The implanted profile is described by the Gaussian function,

$$C(y) = C_{\max} \exp\left\{-\frac{1}{2} \frac{(y - R_p)^2}{\Delta R_p^2}\right\} \quad (1)$$

where C is the concentration, y is the distance from the entrant silicon surface, R_p is the range and ΔR_p is the straggle for the implant. The peak concentration, C_{\max} , is related to the implant dose, Q_{imp} by:

$$C_{\max} = Q_{\text{imp}} / \sqrt{2\pi} \Delta R_p \quad (2)$$

Redistribution data has been generated for the following conditions: [1.1]

Q_{imp} :	5×10^{12} , 10^{13} , 5×10^{13} , 10^{14} cm ⁻²	
R_p :	0.2735 μm	80 keV boron implant.
P :	0.1727 μm	150 keV phosphorus.
ΔR_p :	0.0665 μm	80 keV boron implant.
P :	0.0440 μm	150 keV phosphorus.

The doses are light to moderate resulting in concentrations no heavier than 6×10^{18} cm⁻³, and the range-straggle values are typical of those employed at MSFC. It is assumed that all of the ions become activated shortly after redistribution begins and thereby diffuse by a substitutional mechanism involving vacancies.

b.) Oxidation model: The oxidation model is assumed to be the same as for bulk silicon and the data of Deal et. al. [1.2] has been used to calculate the oxidation rate according to:

$$\frac{dx_o}{dt} = B / (2x_o + B/C) \quad (3)$$

where B and C follow Boltzmann-like temperature dependences. Figures (1) and (2) illustrate the oxide thickness dependence upon time and temperature for both dry O₂ and steam ambients.

During the oxidation, the silicon film thickness is reduced according to:

$$W = W_o - \alpha x_o \quad (4)$$

where W_0 is the initial film thickness, taken to be $1 \mu\text{m}$, and $\alpha = 0.45$ is the ratio of the densities of SiO_2 to silicon. Redistribution data is given for $W_0 = 1 \mu\text{m}$ and an initial oxide thickness of $x_0 = 300 \text{ \AA}$.

c.) Diffusivity model: The diffusivity model for boron was discussed in an earlier report [1.3] and it includes a linear dependence of the diffusivity upon the vacancy concentration as well as the field-enhancement effect. The diffusivity model for phosphorous includes only the field-enhancement effect which is sufficient to describe the non-linear behavior of phosphorous diffusions at concentrations lower than 10^{19} cm^{-3} as shown by Barry [1.4] and Fair and Tsai [1.5]. The diffusivity temperature dependence is after Fair [1.6] and Fair and Tsai [1.5] adaptation of data by Ghostagore [1.6]. For either boron or phosphorous the effective diffusivity is given by:

$$D_{\text{eff}} = D(u) \times (1 + u / \sqrt{u^2 + 1}), \quad (5)$$

where,

$$u = C/2n_i, \quad (6)$$

and,

$$D(u) \approx D_B^* u, \text{ for boron,} \quad (7)$$

$$\approx D_P^*, \text{ for phosphorus.} \quad (8)$$

and where n_i is the intrinsic carrier concentration at the diffusion temperature and D_B^* and D_P^* are the intrinsic diffusivities of boron and phosphorus:

$$D_B^* = 3.17 \exp (-3.59\text{eV} / k_B T) \text{ cm}^2/\text{sec.},$$

$$D_P^* = 3.85 \exp (-3.66\text{eV} / k_B T) \quad (9)$$

B. Further Program Development

The program which was used to generate the data has been described in detail in an earlier report. It was noted that the program was developed in such a way that one could take advantage of a normalization procedure for predeposition diffusions and generate data applicable to different film thicknesses. However, it is not possible to gain such an advantage for redistribution diffusions involving ion-implants or growth of an oxide. Then the program was used to generate data, it was discovered that some other features of the program are extraneous unless further refined.

The program was developed to account for both thin and thick oxides such as would be encountered in some practical situations. However, such a simulation requires the incorporation of a warped grid system, a modification which would require considerably more effort. Therefore, the variable oxide feature is of limited value at this time, since the program, at best, only approximates the conditions for growth of a very thin oxide during redistribution.

A modification was made which allows accurate treatment of redistribution under oxidizing conditions when only a single oxide thickness is involved. The original program treated the oxidation process with regard to the boundary conditions; however, unlike the case of bulk silicon, one must also account for the reduction of

the silicon film thickness. This feature is now included in the program. During the simulation of a redistribution in an oxidizing ambient, the vertical grid spacing continuously shrinks while the horizontal grid spacing is constant. The modification does not show up on logic flow diagrams at the level of detail which has previously been given. For completeness, a new listing of the affected main and sub-programs is given in Appendix C.

C. Computational Procedure

The program described in an earlier report, and modified as described in the preceding, was used to generate the data. Two-dimensional data was obtained in the form of isoconcentration contours for typical situations. The bulk of the data which can be correlated with experimental measurements is generated using a quasi-one-dimensional model in a manner described in a previous report. [1.3] A brief review of the procedure is given in the following.

For generation of sheet resistance, junction depth and integrated impurity dose data as a function of time and temperature, only a one-dimensional profile need be calculated. This is accomplished by making the horizontal grid only three units wide but keeping the field six film thicknesses wide. Periodic boundary conditions for the horizontal dimensions are employed in the program and result in a calculation which produces the vertical profile equivalent to a none-dimensional model. Thus without sacrificing the generality of the program for treating

two-dimensional cases, the amount of computing time is drastically reduced when the data that is desired does not require the full power of the program.

The vertical grid varies from thirty one to sixty one points as required for accuracy in details of the profile, and most of the data is not sensitive to the number of grid points used if the number is chosen in this range. For the purpose of illustrating the unusual nature of phosphorous profiles, the larger number of points was required.

D. Discussion of Results

First, some of the unusual behavior of redistribution diffusions in SOS films will be discussed in this section. Next, the format for the calculated curves will be discussed, and, finally, the bulk of the generated data is given in Appendix A and B without further comment.

Figures (1) and (2) illustrate the oxide thickness growth and silicon film thickness reduction as functions of time for <111> silicon films oxidized in steam and dry O_2 ambients. The evolution traced beginning with an initial oxide of 300 Å thickness on an SOS film of 1 μm initial thickness. The curves are shown for four temperatures. The data are necessary for interpreting some of the results for simulated redistributions.

Figures (3) and (4) show impurity profiles for boron and phosphorus implants being redistributed in a steam ambient at 1000 deg. C. The profiles are all plotted with a common origin as

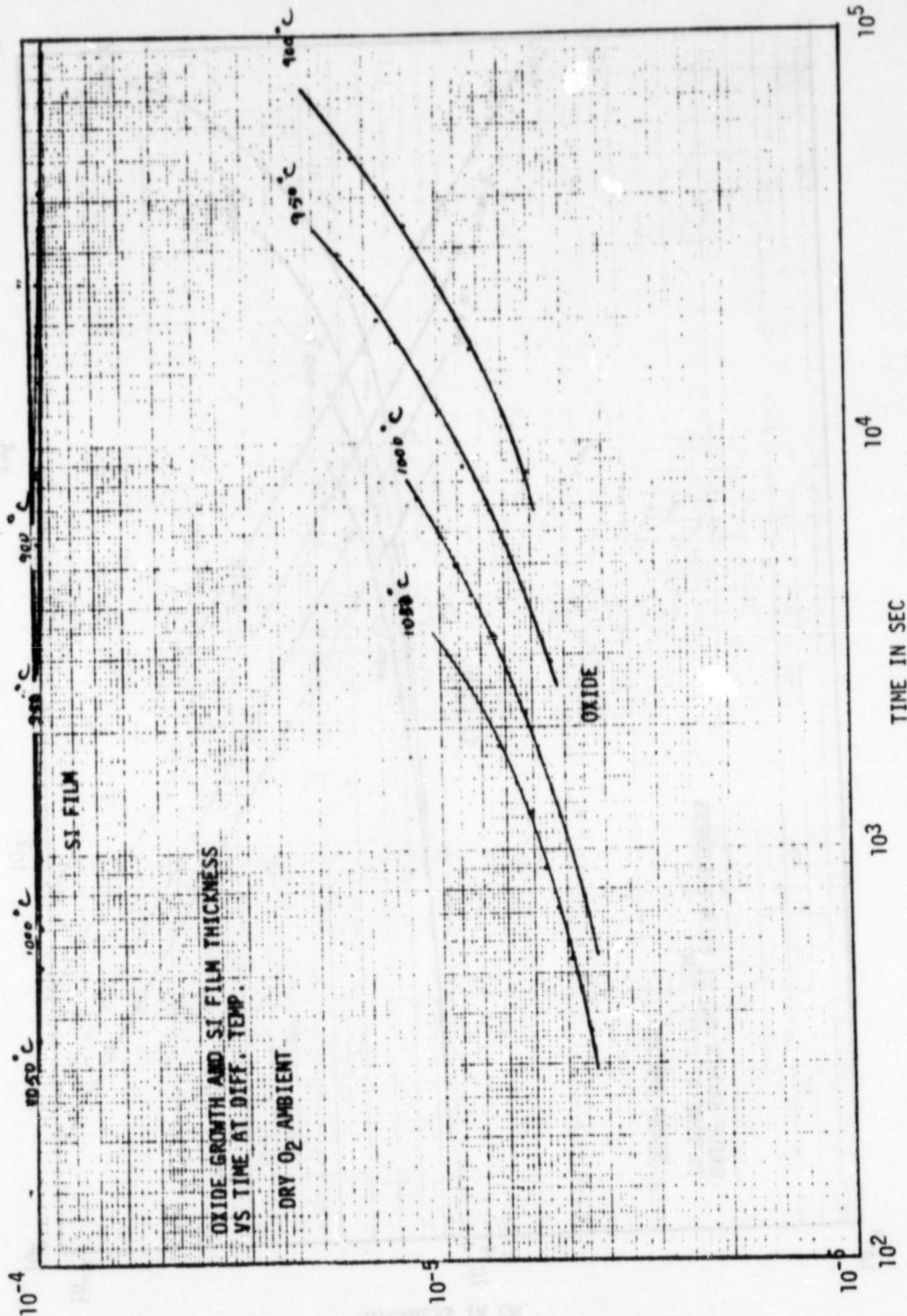


Figure 1.

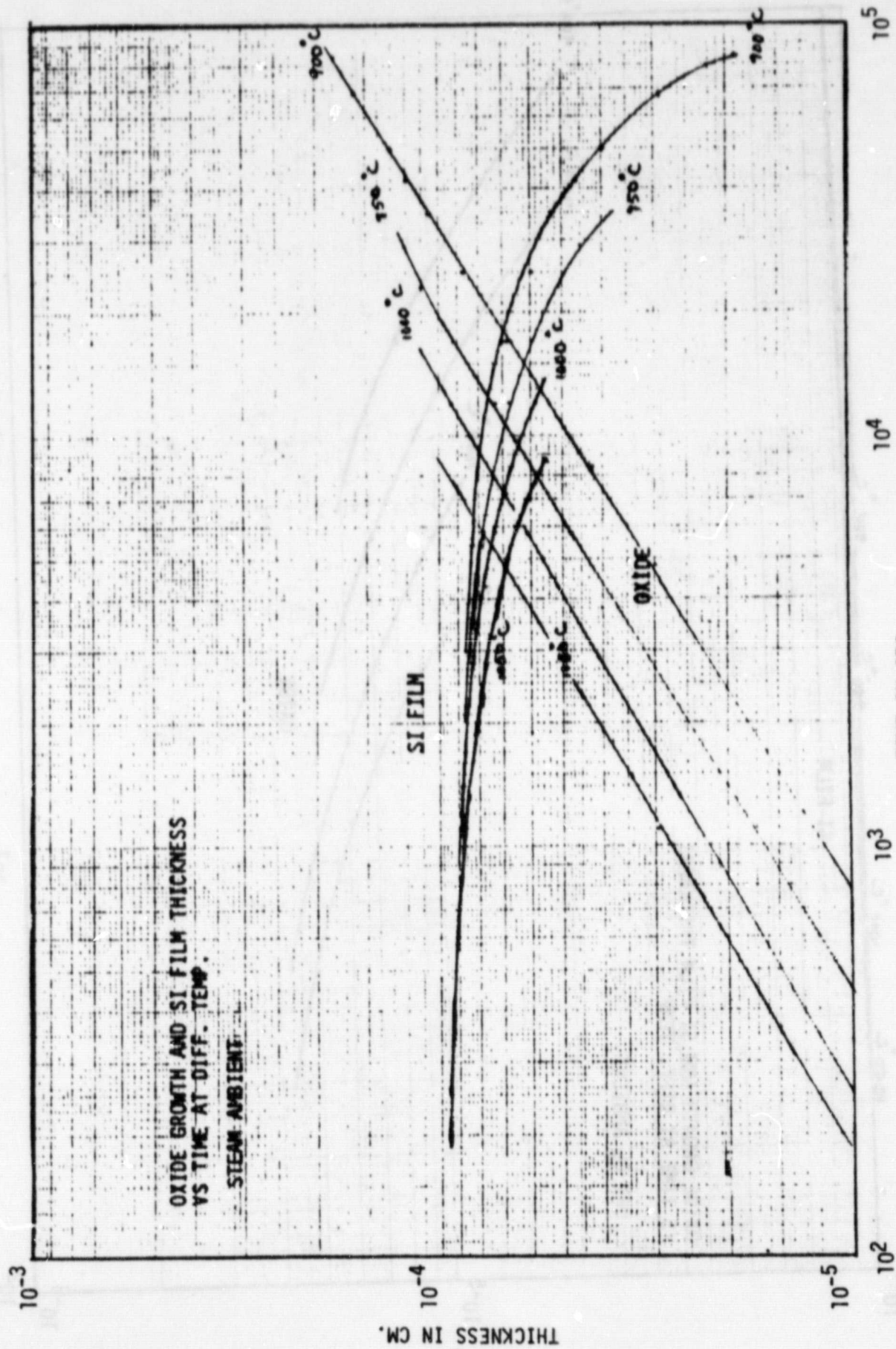
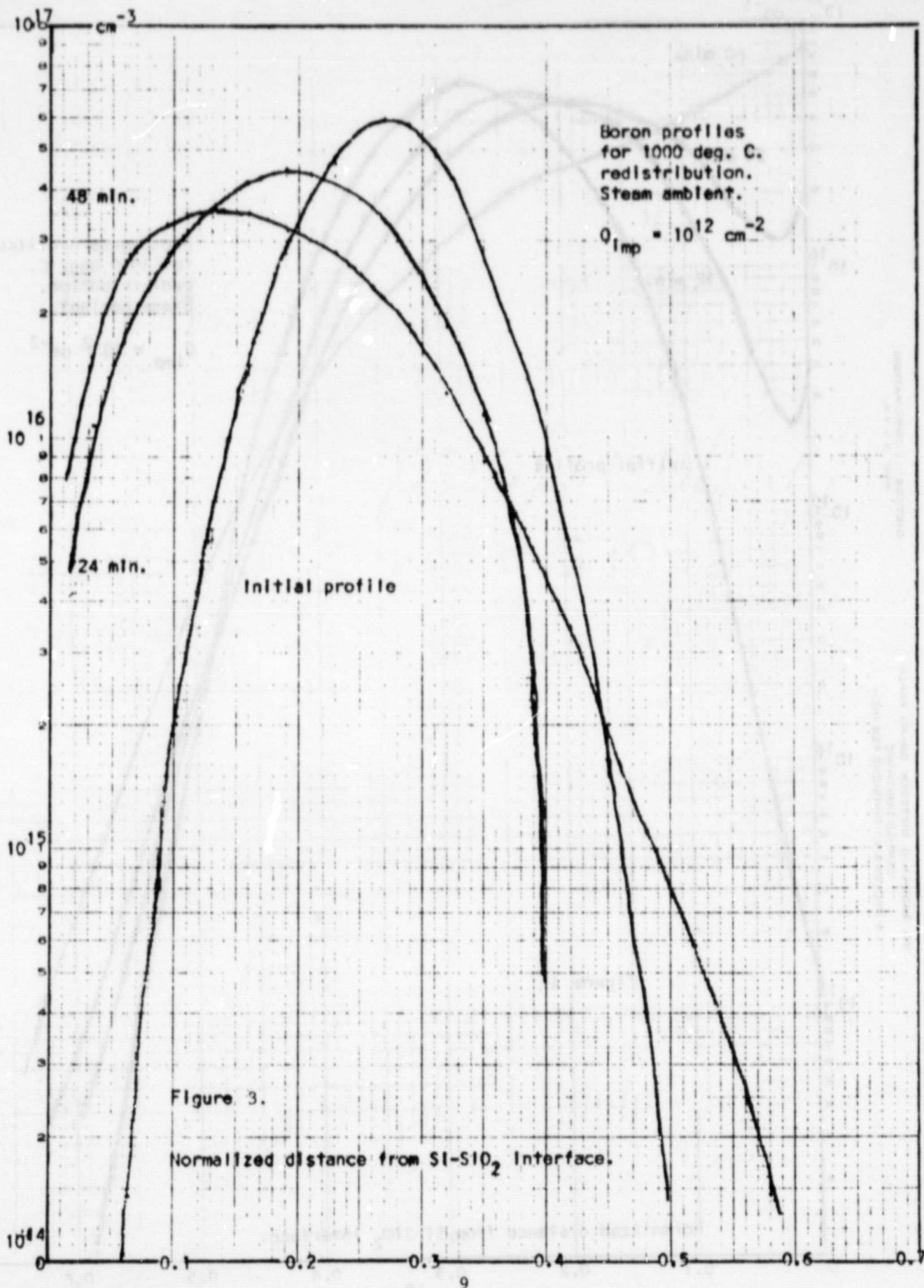


Figure 2.

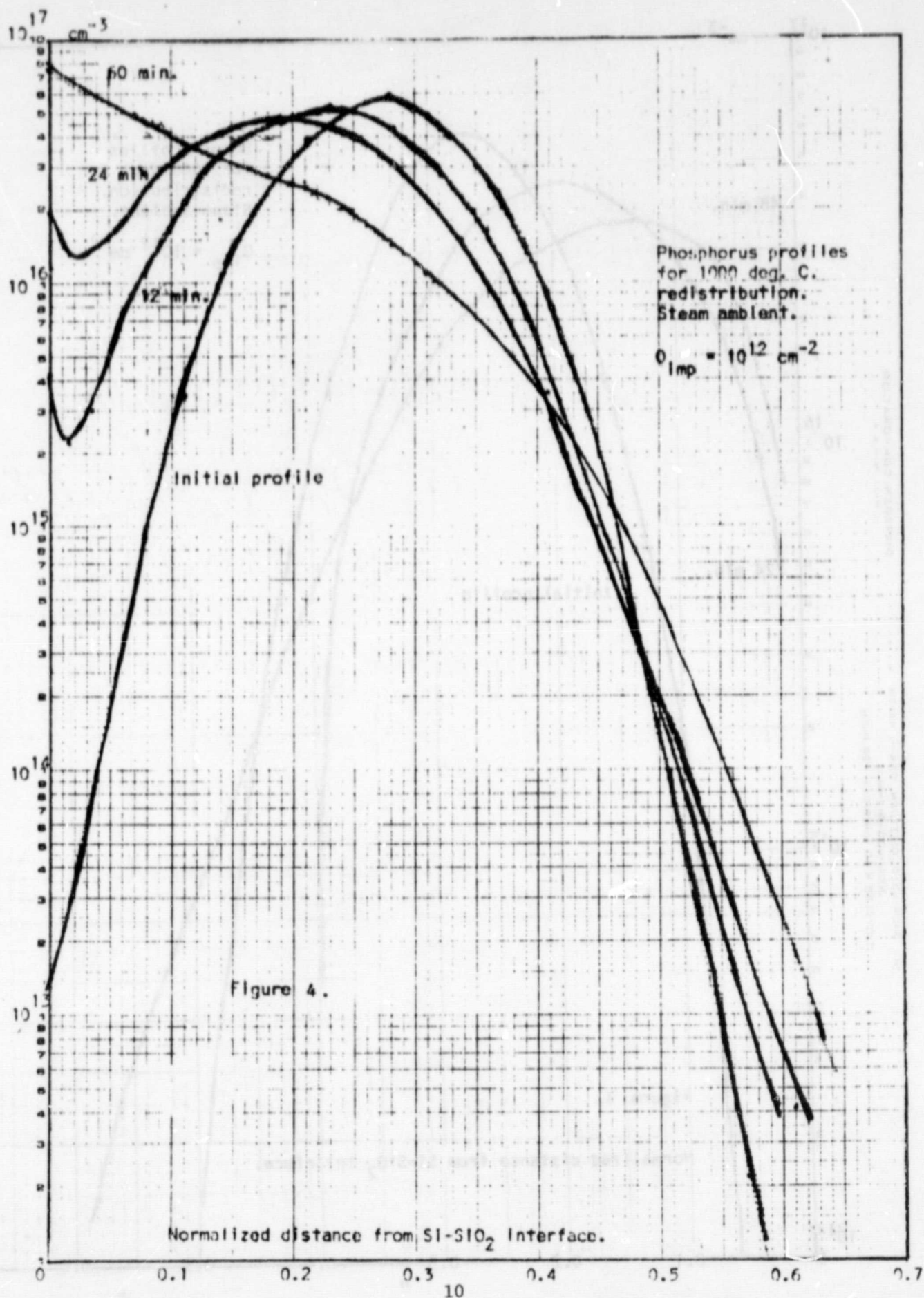
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would be the case for experimentally derived profiles where the Si-SiO₂ interface would serve as the logical origin. However, the profiles are normalized with respect to the film thickness which is of course shrinking. The boron profiles are not unusual but show the wellknown leaching effect due to segregation into the oxide. The phosphorus profiles show the effect of impurities being rejected from the oxide. There is a pile-up of impurities in front of the advancing Si-SiO₂ interface and then a dip which eventually disappears. It is easy for one to draw an erroneous conclusion from observing the profiles, because it appears that the integrated dose should increase or at least remain constant and the sheet resistance should decrease with time. This is not true. Although the segregation coefficient favors phosphorus in silicon vs. SiO₂, eventually all of the phosphorus will be in the SiO₂ when the SOS film is completely oxidized since the model assumes that there is no diffusion into the sapphire.

Figures (5-7) illustrate the behavior of the junction migration, sheet resistance variation, and integrated impurity dose variation over a long period of time. All of the curves are plotted with respect to normalized time, and true time is obtained by multiplying by the normalizing time value given on the plot. Junction depths are in microns, sheet resistance values are in ohms, and dose values are in cm⁻² units unless otherwise marked. The curves are given in the typical format for all of the data.

For an ion-implanted profile, there are in fact two junctions until one of the junctions emerges at the Si-SiO₂ interface.

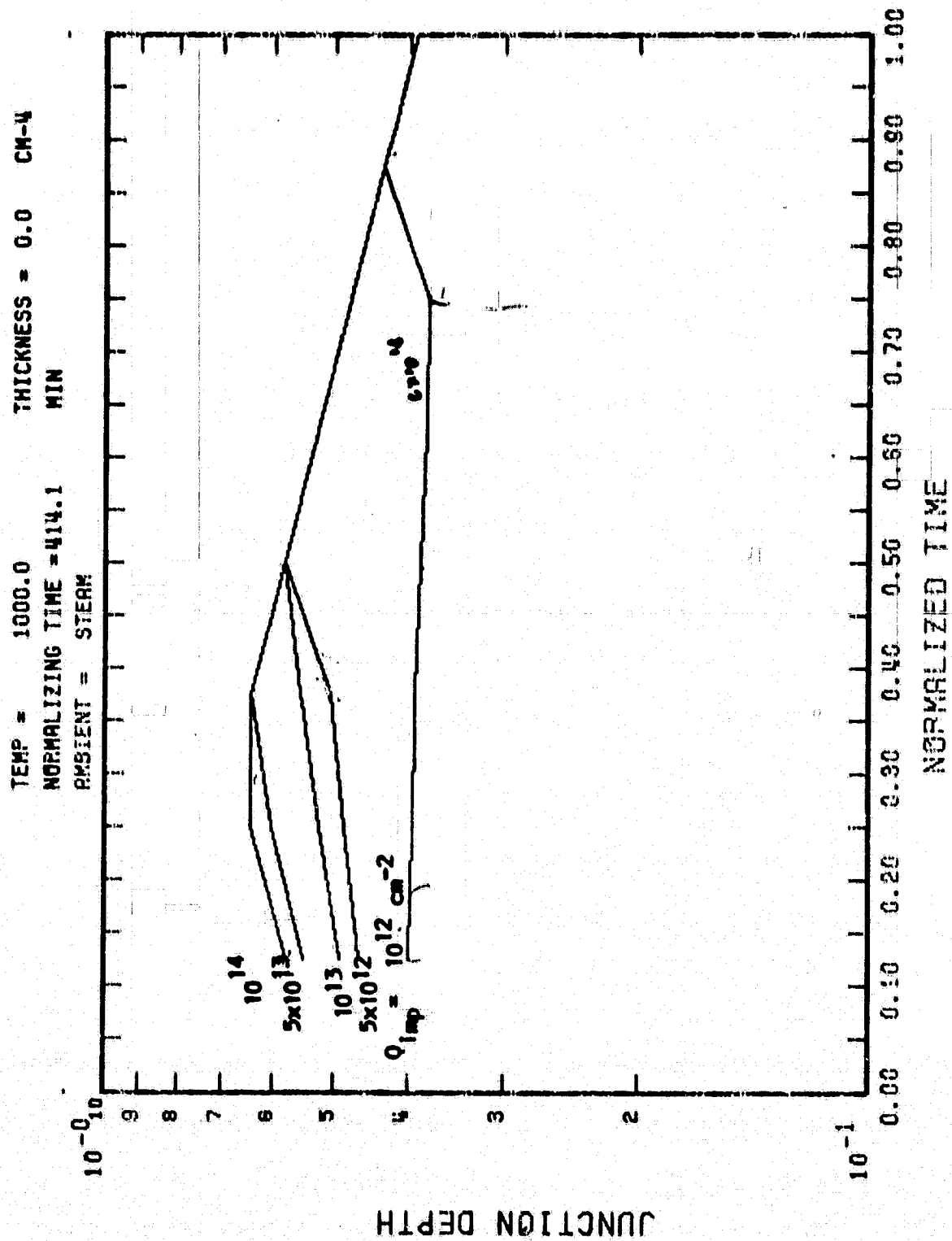


Figure 5. Junction position with respect to Si-SiO₂ interface for Boron redistribution.

TEMP = 1000.0
 NORMALIZING TIME = 414.1 MIN
 AMBIENT = STEAM

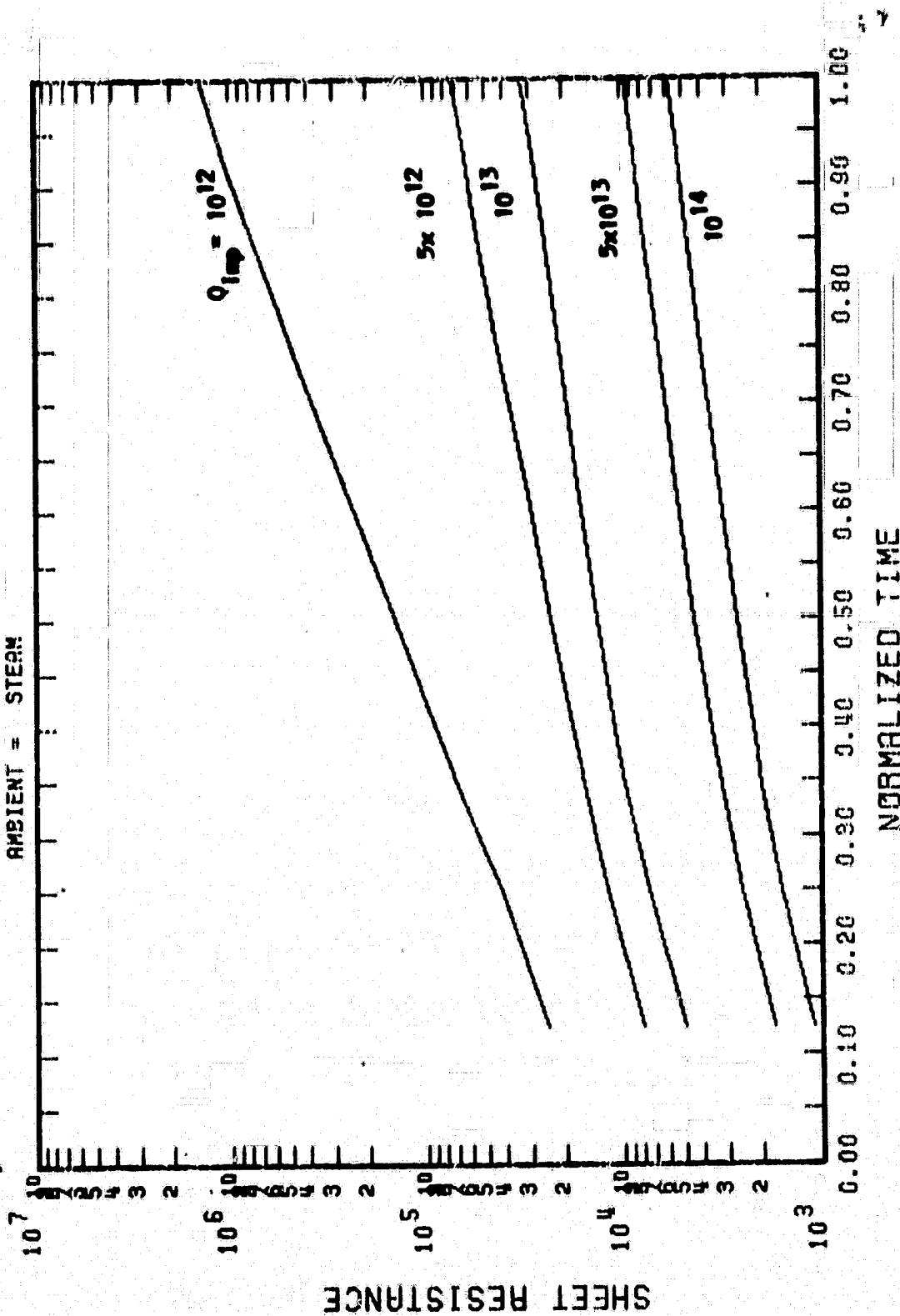


Figure 6. Sheet resistance for Boron redistribution.

TEMP = 1000.0
 NORMALIZING TIME = 414.1 MIN
 AMBIENT = STEAM

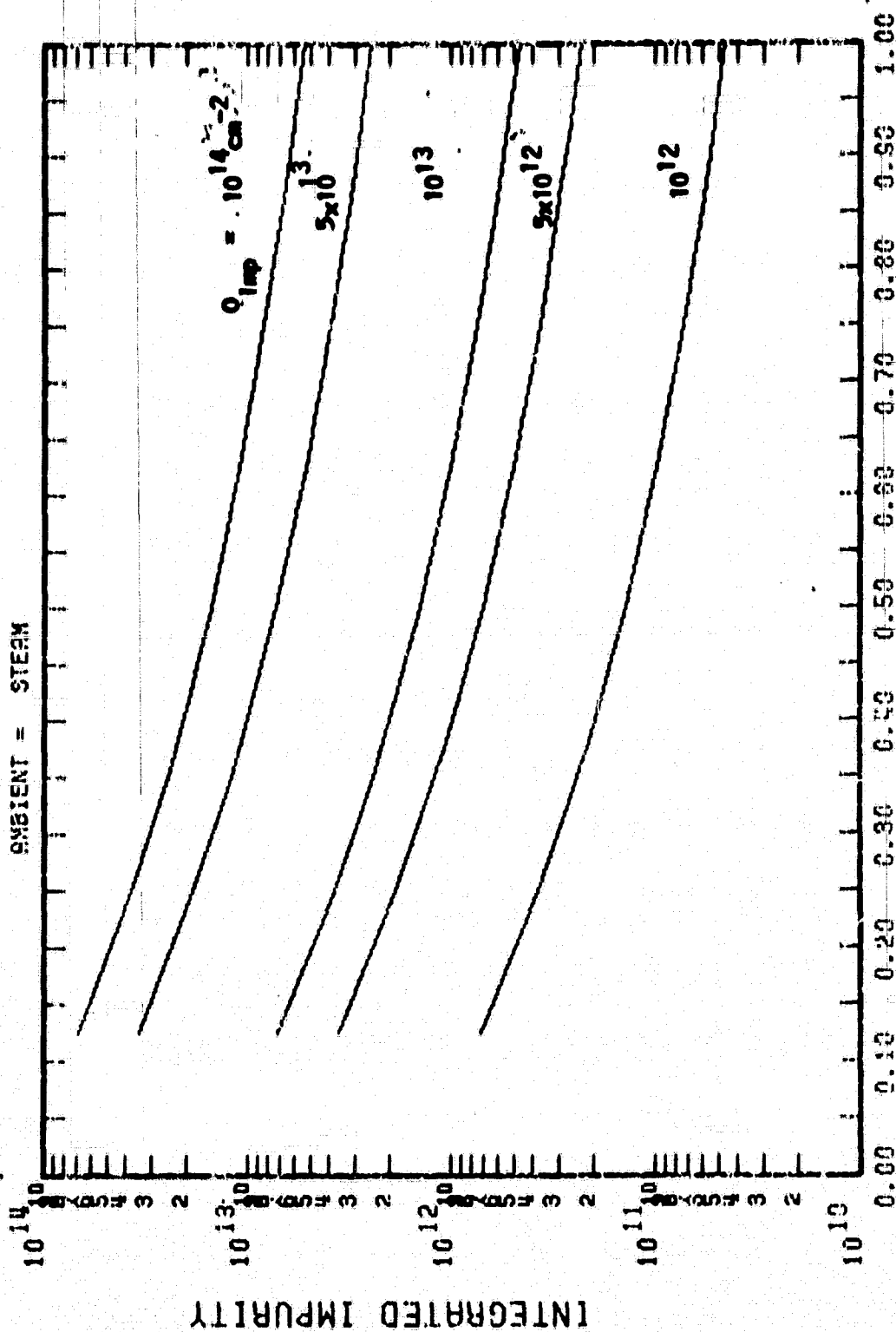


Figure 7. Variation of Dose for Boron redistribution.

Therefore, the sheet resistance values are for the buried layer until the front junction disappears. This typically occurs in a short time compared with that for through-diffusion of the back junction. Figure (5) illustrates the through-diffusion of the back junction for the heavier doses. This always occurs for redistribution in a nitrogen ambient but not necessarily so for an oxidizing ambient. After the through diffusion, or even before for light doses, the junction depth will eventually decrease due to the reduction of the film thickness or due to the relatively slow advancement of the junction with respect to the moving Si-SiO₂ interface. In some of the data presented in the appendix, the junction appears to remain almost stationary for this same reason. The variation of the sheet resistance and dose with redistribution time also may appear strange when compared with results for bulk silicon; however, consideration of the previously mentioned factors also explains these results.

Two-dimensional isoconcentration contours are given in the appendix for the various ambients and the two impurity types. The results are not as remarkable as those given in the last report which were for chemically predeposited boron. In that case, there was initially a heavy concentration of fast diffusing impurities at the Si-SiO₂ interface which were strongly retarded due to the segregation phenomena. This does not happen with the ion-implanted predeposit because the initial profile lies below the interface at which the segregation phenomena is effective.

II. DOUBLE-LEVEL METALLIZATION TECHNIQUES

A. Long Term Objective

Integrated circuit technologies which incorporate two-levels of metallization into the interconnection scheme are often limited in density and yield because of limitations in the double-layer metal technology itself. With a dual level aluminum and deposited (low temperature) silicon oxide as the base system, the primary objective of this program is to evaluate the basic yield limitations of that system and investigate alternate approaches in order to enhance the yield and/or facilitate improved circuit density. With the pressure of device (or design rule) scaling as an on-going philosophy, high yield for a large number of small vias and small lines becomes extremely important.

B. Fabrication Facilities at Mississippi State University

Most of the facilities work during this contract period was directed toward the development of a sputtering system for preparing aluminum and aluminum-alloy films in support of the double layer metal program. A photograph of the completed system is shown in Figure 8. Briefly, the system consists of the following.

The basic vacuum system is a Varian-NRC 6 inch oil diffusion and mechanical roughing pump equipped for automatic and manual operation. The diffusion pump is equipped for LN_2 cooling of the

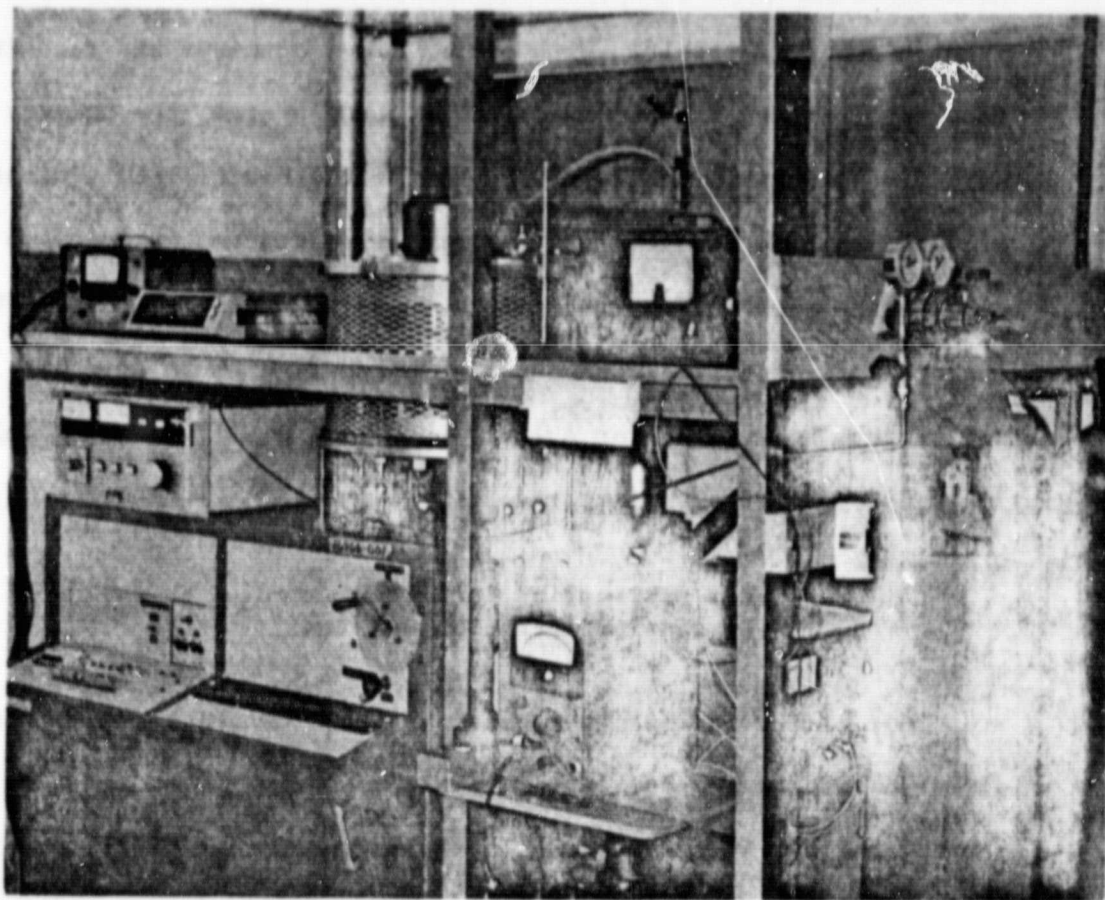


Figure 8. Photograph of metallization system using sputter-gun source.

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cold trap. The sputter gun and power supply were obtained from Sloan Technology. The sputtering chamber was designed and built at Mississippi State. It consists of a Corning 12x18 glass cylinder and an aluminum top plate machined to accommodate up to three sputter guns. A cold cathode discharge gauge was constructed and installed in the baseplate of the chamber to measure the pressure during the sputtering operation. A throttle valve with several threaded holes for accommodating plugs is operated by one of two mechanical feedthroughs in the baseplate. A lift mechanism with a reversible motor was designed and constructed for raising the top plate and sputter guns.

Inside the chamber is equipped with a rotating table which accommodates up to eight wafers of 1½-2" in diameter. The table is driven by a vacuum sealed shaded pole motor through a magnetic coupling at 7 rpm. The entire motor-table assembly is rotated by a chain-sprocket-mechanical feedthrough arrangement through three sputter-gun and two mask positions. The mask is attached to the rotating assembly and provides one hole through which the sputter-gun deposits metal on the wafers. A crystal film thickness sensor is located beneath the sputter-gun and receives a deposit through a hole at an unused wafer position on the table.

The sputtering chamber opens into a class 100 clean bench in order to maintain a high level of cleanliness. The system is located in the metallizing and bonding room of the microelectronics laboratories in Simrall Engineering Building, and this room was designed with air conditioning and filtering units to maintain a class 10,000 environment.

The installation of a six-tube Thermco Ranger diffusion furnace was completed with the addition of a venting system for exhausting the scavenger boxes.

Complete PMOS circuits have been fabricated in the MSU facilities.

A summary of the microelectronics facility at MSU is provided in Appendix E.

C. Double Layer Metal Experiments

Reviewing the literature has disclosed many investigations relative to the surface oxidation processes of aluminum, including recent reported results by Bell Lab personnel which directly relates to double layer metal processing. These studies show that the aluminum surface is extremely reactive and grows $\text{Al}_2\text{O}_3 \cdot n\text{H}_2\text{O}$ films rapidly in water based solutions to thicknesses which cannot be reduced during the sintering operation. Even the growth rate of Al_2O_3 on Al in air at room temperature is reported to be in the range of 30 \AA . This compares with the Bell Lab's estimate of 55 \AA of Al_2O_3 which can marginally be reduced by sintering.

After careful review of the basic double layer metal process, certain ones stand out as suspect: (1) The via etch using buffered etch, (2) the initial oxidation during vapox deposition, and (3) the photoresist removal.

Consequently, three sets of experiments were initiated:

- 1) modification of the wet chemistry techniques,

2) dry chemistry processing and/or new insulation materials, e.g., polyimide, nitride,

3) the incorporation of in situ back sputtering.

Dramatic improvements in yield were achieved with relatively minor changes in the wet chemistry processing. The effective yield in the number of vias having a total contact resistance of less than 500 ohms has been increased to the 98-99 per cent level for a test pattern having 560 vias of varying sizes by the use of wet chemistry processing techniques and post-heat treatments. Alternations in the process which accounts for these results consists of the following:

1) etching the vias (intermetal contact windows) through C.V.D. - SiO_2 using an ultrasonic etch process in the dark has rendered improved results over that whereby etching was accomplished by dipping the wafer in stirred B.O.E.

2) chemically cleaning the first level metal through the vias with 1:1:1 ethylene glycol: buffered HF: H_2O solution for 20-30 seconds just prior to depositing the second level metal.

3) the use of phosphorus doped vapox to allow for faster via etch times and the ability to perform post heat treatments of temperatures in the 500°C . range without the cracking (crazing) observed with undoped vapox. The use of phosphosilicate glass also tends to give a lower initial contact resistance over that obtained with undoped vapox.

4) the use of post heat treatment (sintering) in the vicinity of 500°C . tends to drastically decrease the total via contact

resistance thereby increasing yield. On wafers exhibiting initial poor yields, sintering can improve this yield by 500-800 percent. On wafers having good yield initially, the contact resistance can be substantially improved. (Average contact resistance of 150 and 200 ohms have been obtained for 560 vias of 0.5 and 0.2 mil square vias, respectively.)

The details of these double layer metal experiments relative to wet chemistry have been reported in a special report, but are included for convenience in Appendix F, "Sintering Effects on Double Layer Metal for VLSI Applications".

The exploratory processing involving dry chemistry required the use of plasma etching and plasma deposition equipment not available at either the Marshall Space Flight Center or Mississippi State University. Consequently, the logistics involved in processing the wafers have been difficult.

Four types of insulators were to be investigated:

- 1) 5% phosphorus doped silox,
- 2) plasma nitride,
- 3) the GAF version of polyimide, and
- 4) the Hitachi PIQ.

Whenever possible, dry chemistry processing was to be compared with "standard" wet chemistry. The wafers were processed through the first metal mask at Marshall Space Flight Center in standard fashion. The polyimide material was processed at American Microsystems, Inc. (AMI) using the standard recommended procedures by

the manufacturees. The nitride and silox were deposited at AMI using their standard processes, the former on an Applied Materials plasma reactor. The wet chemistry processing was performed at AMI using AMI's standard processing. The plasma etching was performed by Davis and Wilder on one of their production parallel plate plasma system using their proprietary processes.

The wet chemistry split involving silox was lost when the standard "pad" etch attacked the metal completely. The same batch etchant continued to provide good results on AMI material. Since the first layer metal at NASA was deposited via sputtering and with many different impurities, compared with approximately 1% Si:Al deposited with electron beam, the difference in the metal film is believed to be the source of the problem.

The plasma nitride material and silox material, deposited by AMI and plasma etched by Davis & Wilder, was processed without any problems other than long delays. This material plus the polyimide material has finally been received for the final processing here. Although, no electrical results are available at the present, the microscopic examination displays the expected sharper edges of the dry processed material vs. the standard wet chemistry.

In the meantime, the results of the in situ back sputtering experiment were obtained. As was expected, the in situ back sputtering split gave much improved yields over that for the standard material - the detail results being published elsewhere.

The results of these experiments points to the requirement to

very effectively remove the Al_2O_3 prior to the second metalization or minimize its formation during wafer processing to within the order of 30 \AA which a good sintering treatment can reduce. The in situ cleaning forgives prior processing which tends to grow the Al_2O_3 such as photoresist removal and buffered HF etching of oxide.

The dry processing has the potential in the future of resolving smaller via sizes and, simultaneously, avoids the harmful H_2O to accelerate the aluminum oxide (and hydrate) formation. Although dry processing to remove the photoresist is routinely done one should expect Al_2O_3 formation due to the presence of active oxygen in the "ashing" process. Some parallel plate reactors can be modified to introduce Ar at low pressure and effectively as in a back sputtering mode. This latter mode could then be used as a clean up step prior to second metal deposition - although not in situ. Undoubtedly, dry processing is going to be extremely important in future double layer metal development work.

III. TWO-DIMENSIONAL MOSFET SIMULATION PROGRAM

A. Long Term Objective

The basic long term objective is to develop a two-dimensional computer program which derives the channel current in steady-state from given values of potential; source, drain, gate, and substrate. Also given are physical parameters such as gate length, dielectric thickness, doping levels, etc. The substrate doping level should be variable in two dimensions and the substrate potential is independent of the source potential in order to include body-bias effects. The program is intended to model MOSFETs with short channels with particular emphasis on subthreshold and punch-through conduction.

Secondary objective is to utilize techniques in the computer program to minimize computer run time while still maintaining reasonable simulation accuracy.

B. Scope of Work

Review the literature dealing with electrical models for the MOS transistors which takes into account two dimensional effects and investigate their applicability to short channel structures. Identify and demonstrate computer methods suitable for analysis and investigate preliminary problems which need to be solved.

C. Introduction

At the beginning of this project no programs were available which satisfied the specified objectives. There has been considerable work in two-dimensional modelling of JFETs including the works of Kennedy and O'Brien [3.1] and Martin Reiser [3.2]. The MESFET has also received attention in two-dimensional simulation, e.g., Barnes [3.3]. Various modes of MOSFET operation have been simulated or modeled using two-dimensional techniques, e.g. Schroeder and Muller [3.4] (saturation), Barron [3.5] (low level currents), Armstrong et al [3.6] (pinch-off), Kennedy [3.7] (effects of ionizing radiation), Kennedy and Marley [3.8] (saturation), Mock [3.9], Motta [3.10], El-Mansy and Boothroyd [3.11]. Although these works all contribute to the knowledge required in reaching the objective of this task, only the effort by Mock is sufficiently general to meet the objectives--and it is unavailable for public distribution.

The work by Barnes [3.3] described the application of the finite-element method to the analysis of the MESFET.

Further, the finite-element method has been used for some time in solving problems in mechanics and elasticity; however, it has only recently been applied to semiconduction problems. This method has the power to treat some problems, such as eigen-value problems, for which the finite-difference method is awkward if at all applicable. It can also be applied to the solution of field

distributions governed by partial differential equations, and one of the most attractive features as compared to the finite-element method is purported to be the ease of treating non-rectangular geometries and irregular boundaries. For example, the geometry of the VMOS structure could be accommodated. It was decided to further investigate this technique.

The details of this evaluation are included in the appendix. In summary, the evaluation resulted in some skepticism that the finite element method would be sufficiently effective for semiconductor problems to justify the effort. A more recent paper has reinforced this attitude. This paper indicates that the proper formulations of the semiconductor problem for the finite element approach remain to be demonstrated, and, in agreement with our observations, point out that the application of Galerkin's method is subject to skepticism. Therefore, it was concluded that the further work should be based upon the finite-difference method which we have used before although the finite-element method is intriguing and may be further developed in the future.

Key in the development of this task is the proper selection of assumptions. Certain assumptions are required to focus the effort and facilitate convergence expeditiously and, therefore, minimize computer time. On the other hand, too many assumptions lead to loss in utility.

The basic assumptions follow:

- 1) Recombination/generation is negligible.
- 2) Hole conduction is negligible.

3) The conventional expression for Poisson's equation is valid [see next section].

4) The mobile majority carriers are included in an infinitesimally thick layer of charge at the Si-SiO₂ interface.

5) The current flow in the channel is then described by a one-dimensional equation,

$$J_n = qD \frac{\partial S}{\partial x} + q \mu_n S E_x$$

where

S = density of majority carriers in the channel,

D = majority carrier diffusion constant,

μ = channel carrier mobility, and

E_x = tangential electric field component.

The first three sections are common in the stated literature and restrict the model from covering phenomena associated with breakdown and bulk generated leakage currents. The last assumption is key and separates this work seriously from that of Mock although Kennedy [3.7] used a similar approach for the sake of simplification.

Key also are the normal assumptions which are not made and which are commonly utilized:

- 1) the gradual channel approximation,
- 2) constant substrate doping, and
- 3) zero substrate bias.

Although a constant effective channel mobility is utilized during the initial development of the program, it is not intended to remain a basic assumption.

Assuming step junctions at the source (or drain), the potential in the depletion region and oxide is defined by Poisson's equation with appropriate boundary conditions (Figure 9):

- 1) fixed potential along the source (or drain) boundary (BCD and IJK),
- 2) fixed potential deep within the bulk substrate (AL),
- 3) zero horizontal component of electric field under the source and drain and far from the channel (AB and KL),
- 4) zero horizontal component of electric field in the oxide far from the channel (EF and KH) and
- 5) constant potential on the gate electrode (FG).

For convenience the substrate in the basic program is defined as having zero potential. The source, drain, and gate potentials are their respective applied potentials plus their work functions with respect to the substrate, i.e.,

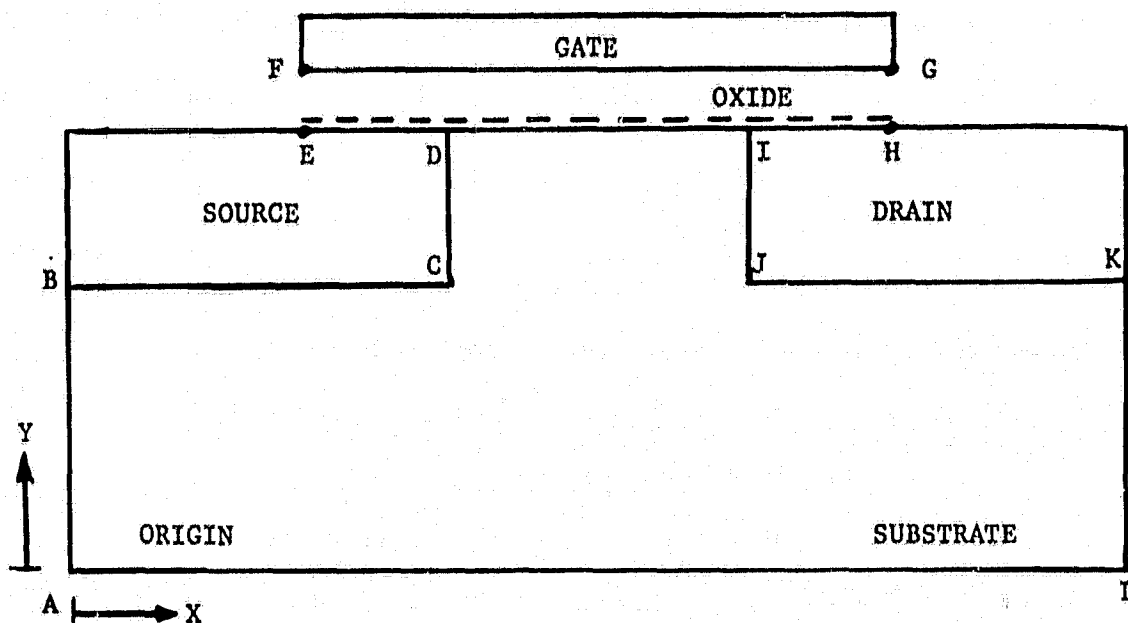
$$\psi_{\text{source}} = V_S + V_{Bi} ,$$

$$\psi_{\text{drain}} = V_D + V_{Bi} ,$$

$$\psi_{\text{gate}} = V_G + \phi_{ms} .$$

For the NMOS example the potential ψ is always non-negative.

The gate dielectric is assumed to be ideal with infinite resistivity. The charge density in the dielectric is assumed to be zero except for a sheet charge representing the silicon-silicon dioxide interface charge Q_{ss} which is arbitrarily assumed to be $50 \text{ } \overset{\circ}{\text{A}}$ within the oxide at one grid spacing above the channel grid.



DISTANCES

$$AB = YDIST - YDIF$$

$$CD = JI = YDIF$$

$$EF = HG = TOX$$

$$BC = JK = XDIF$$

$$AL = XDIST$$

OTHER RELATIONSHIPS

$$IK5 = 1K-5, IL5 = IL + 5$$

$$JL\phi = JL-1, JK = JK1-1$$

$$JMAX1 = JMAX + 1$$

$$JMAX\phi = JMAX-1$$

CO-ORDINATES

$$A = (1, 1)$$

$$B = (1, JK1)$$

$$C = (IK, JKI)$$

$$D = (IK, JMAX)$$

$$F = (IK5, JL)$$

$$G = (IL5, JL)$$

$$I = (IL, JMAX)$$

$$K = (IMAX, JK1)$$

$$L = (IMAX, I)$$

Figure 9. MOSFET Gross-Section

Key to the simulation of short channel devices is solving the two-dimensional Poisson's equation without making unnecessary approximations. The finite-difference formulation for Poisson's equation is given in the next section. The majority carrier charge is neglected in this formulation except for the sheet charge representation at the oxide interface. The intent is to ignore the charge where it is negligible compared with the ionized doping charge--which is a good assumption everywhere except in the channel.

One can then solve Poisson's equation for the two-dimensional potential distribution more easily and faster than if the coupled majority carrier current equation is included and the majority carrier density variable is included for every mesh node.

After finding the potential distribution one can, after the fact, explicitly solve for the majority carrier densities and current in order to predict punch-thru and subthreshold conduction behavior. This approach is aimed at minimizing computation time while retaining the essential relationships to maintain sufficient accuracy for modeling purposes. One should expect a compromise in accuracy, under certain conditions, when compared with the more general approach of solving the two-dimensional conduction equation.

D. The Poisson Equation, Difference Form

The Poisson equation in different form is

$$\nabla^2 \psi = - \rho / \epsilon \quad (10)$$

where

- Ψ = electrostatic potential,
- ρ = charge density, and
- ϵ = permittivity of the material.

For acceptor doped material the charge density is

$$\rho = q(p - nN_a) \quad , \quad \text{depletion,} \quad (11)$$

where

- q = charge density,
- p = hole density,
- n = electron density, and
- N_a = ionized acceptor density.

The hole density is defined by

$$p = N_a \exp(-u) \quad (12)$$

where

- $u = q\Psi/kT$, the normalized potential, and
- $u = 0$ in the charge neutral bulk.

Consequently, in the bulk substrate and in the depletion layer where the electron density can be neglected,

$$\rho = -q N_a [1 - \exp(-u)] \quad . \quad (13)$$

In the channel region the assumption is made that the electrons exists only in a sheet form of infinitesimal thickness at the silicon dioxide-silicon interface. Since the hole density is insignificant at inversion, the charge density in the channel is

$$\rho_s = -q(N_{as} + n_s) \quad , \quad \text{channel,} \quad (14)$$

where

N_{aS} is the effective sheet charge due to the ionized acceptors within the grid spacing defined by the interface grid, and n_s is the sheet charge of electrons in the channel.

Near the oxide-silicon interface there are positive interface charges of density N_{SS} , consequently,

$$\rho = qN_{SS} \quad , \quad \text{interface,} \quad (15)$$

with the location being assumed to be 50 \AA inside of the oxide. Otherwise in the oxide the charge is assumed neutral.

$$\rho = 0 \quad , \quad \text{oxide,} \quad (16)$$

To solve the Poisson equation numerically, the left hand side can be expanded in difference form as

$$\begin{aligned} \nabla^2 \psi &= V_T \nabla^2 U \\ &= V_T [A U_{i,j-1} + B U_{i-1,j} + C U_{i,j} \\ &\quad + D U_{i+1,j} + E U_{i,j+1}] \end{aligned} \quad (17)$$

where $V_T = kT/q$,

$$A = 2[h_{j-1}(h_{j-1} + h_j)]^{-1},$$

$$B = 2[w_{i-1}(w_{i-1} + w_i)]^{-1},$$

$$D = 2[w_i(w_{i-1} + w_i)]^{-1},$$

$$E = 2[h_j(h_{j-1} + h_j)]^{-1}, \text{ and}$$

$$C = -(A + B + D + E)$$

with the grid system defined in Figure 10.

Using the charge equation (13) the complete Poisson equation in finite-difference form is written for node (i,j) as

$$\begin{aligned} A(i,j)U_{i,j-1} + B(i,j)U_{i-1,j} + C(i,j)U_{i,j} + D(i,j)U_{i+1,j} \\ + E(i,j)U_{i,j+1} = \frac{qN_a}{\epsilon V_T} [1 - \exp(-U_{i,j})] \end{aligned} \quad (18)$$

The above nonlinear equation can be linearized by defining a function F such that

$$\begin{aligned} F(U_{i,j-1}, U_{i-1,j}, U_{i,j}, U_{i+1,j}, U_{i,j+1}) &= F_{i,j} \\ &= A(i,j) U_{i,j-1} + B(i,j) U_{i-1,j} + C(i,j) U_{i,j} \\ &\quad + D(i,j) U_{i+1,j} + E(i,j) U_{i,j+1} \\ &\quad - (qN_a/\epsilon V_T) [1 - \exp(-U_{i,j})] = 0 \end{aligned} \quad (19)$$

Defining a set of reference value of U 's and F such that

$U_{i,j-1}^r, U_{i-1,j}^r, U_{i,j}^r$, etc. and $F_{i,j}^r$, one can expand F around the

reference potentials:

$$\begin{aligned} F_{i,j}^{r+1} &= F_{i,j}^r + \left. \frac{\partial F}{\partial U_{i,j-1}} \right|_r \Delta U_{i,j-1} + \left. \frac{\partial F}{\partial U_{i-1,j}} \right|_r \Delta U_{i-1,j} \\ &\quad + \left. \frac{\partial F}{\partial U_{i,j}} \right|_r \Delta U_{i,j} + \left. \frac{\partial F}{\partial U_{i+1,j}} \right|_r \Delta U_{i+1,j} + \left. \frac{\partial F}{\partial U_{i,j+1}} \right|_r \Delta U_{i,j+1} \end{aligned} \quad (20)$$

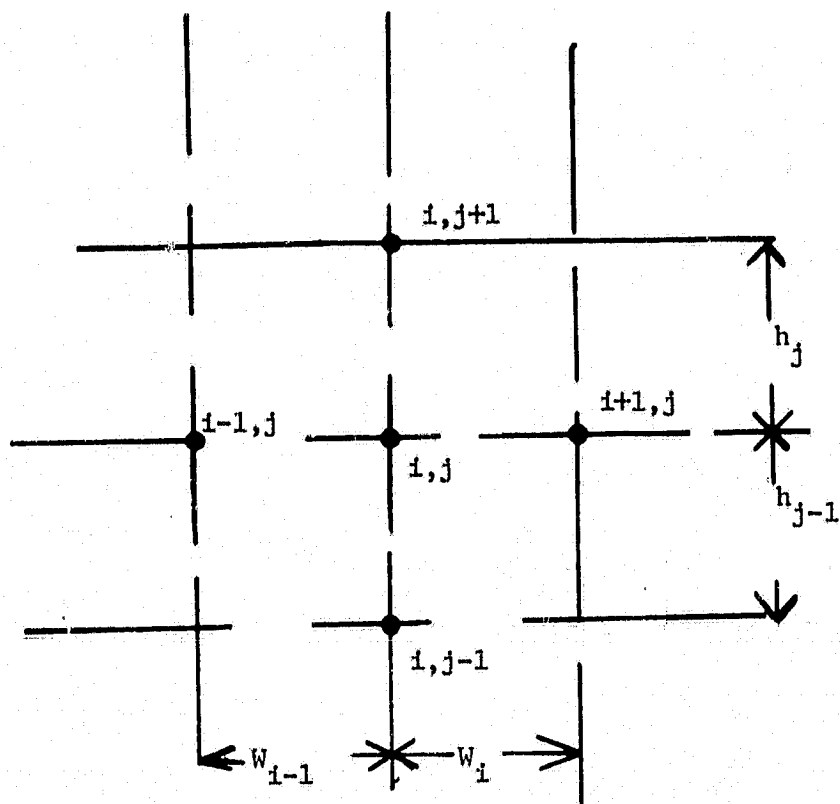


Figure 10. Grid system definition

where

$$\Delta U_{i,j-1}^r = U_{i,j-1}^{r+1} - U_{i,j-1}^r, \text{ etc.}$$

The above expressions defines a system of equations in ΔU as

$$\begin{aligned} F_{i,j}^r = & \bar{A}(i,j) \Delta U_{i,j-1} + \bar{B}(i,j) \Delta U_{i-1,j} + \bar{C}(i,j) \Delta U_{i,j} \\ & + \bar{D}(i,j) \Delta U_{i+1,j} + \bar{E}(i,j) \Delta U_{i,j+1} + F_{i,j}^r \end{aligned} \quad (21)$$

where

$$\bar{A} = A, \bar{B} = B, \bar{D} = D, \bar{E} = E, \text{ and}$$

$$\bar{C} = C - (qNa/kT) \exp(-U_{i,j}^r)$$

with A through E being defined in equation (17). The function F is theoretically zero; therefore, by setting $F_{i,j}^{r+1} = 0$, a system of linear equations in ΔU is obtained. For the node i,j

$$\begin{aligned} \bar{A} \Delta U_{i,j-1} + \bar{B} \Delta U_{i-1,j} + \bar{C} \Delta U_{i,j} \\ + \bar{D} \Delta U_{i+1,j} + \bar{E} \Delta U_{i,j+1} = - F_{i,j}^r \end{aligned} \quad (22)$$

where $F_{i,j}^r$ is defined in equation (19).

By applying the method of lines, the linearized equations are resolved into a tridiagonal matrix form as

$$\begin{aligned} \bar{A} \Delta U_{i,j-1} + \bar{C} \Delta U_{i,j} + \bar{E} \Delta U_{i,j+1} \\ = - F_{i,j}^r - \bar{B} \tilde{\Delta U}_{i-1,j} - \bar{D} \tilde{\Delta U}_{i+1,j} \end{aligned} \quad (23)$$

where $\tilde{\Delta U}$ are taken as the most recent updated values of ΔU each iteration, but still keeping the U 's fixed until convergence

is achieved. The above equation (23) retains the old values of ΔU along the x-axis and calculates the new values of ΔU along the y-axis. Obviously, equation (23) can be written for the inverse case. By alternating between the vertical and horizontal forms of the tridiagonal matrix, the convergence can be expedited.

Special consideration must be given to Poisson's equation at the silicon-silicon dioxide interface. Figure (11A) illustrates the channel sheet charge S in charge per unit area, the acceptor charge N_a in charge per unit volume, and the discontinuity in permittivity. Applying Gauss's law in one dimension with two surfaces at the midway points between C & $C+1$ and $C-1$ & C leads to the expression

$$\begin{aligned} \epsilon_{ox} E_{1/2} - \epsilon_{Si} E_{-1/2} &= \text{positive charge enclosed} \\ &= -q \left(S + \frac{N_a h_{c-1}}{2} \right) \end{aligned} \quad (24)$$

Multiplying through by $\frac{2}{V_T(h_c + h_{c-1})\epsilon_{Si}}$ leads to

$$\frac{2}{h_c + h_{c-1}} \left[\frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{(U_{c+1} - U_c)}{h_c} + \frac{U_{c-1} - U_c}{h_{c-1}} \right] = \frac{Zq}{\epsilon_{Si} V_T} \frac{S + \frac{N_a h_{c-1}}{2}}{h_c + h_{c-1}} \quad (25)$$

which is the one dimension form of Poisson's Law

$$\frac{d^2}{dy^2} \left(\frac{\epsilon U}{\epsilon_{Si}} \right) = - \frac{p_{eff}}{\epsilon_{Si}} \quad (26)$$

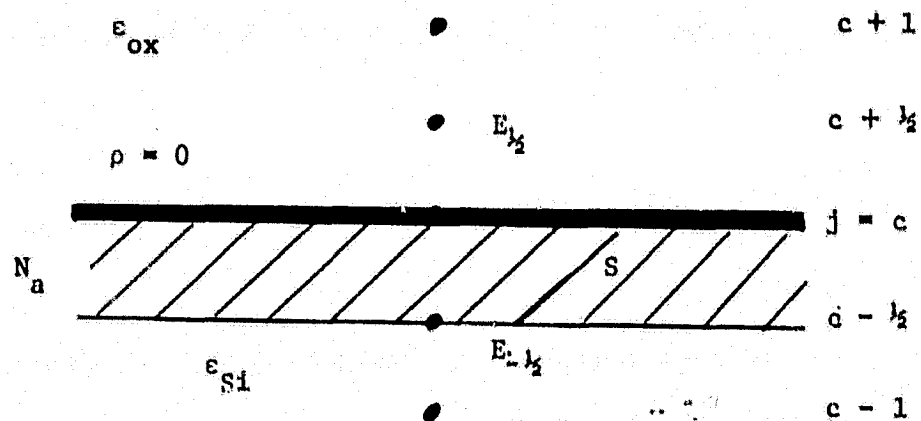


Figure 11A. Gauss's law at the silicon-silicon dioxide interface

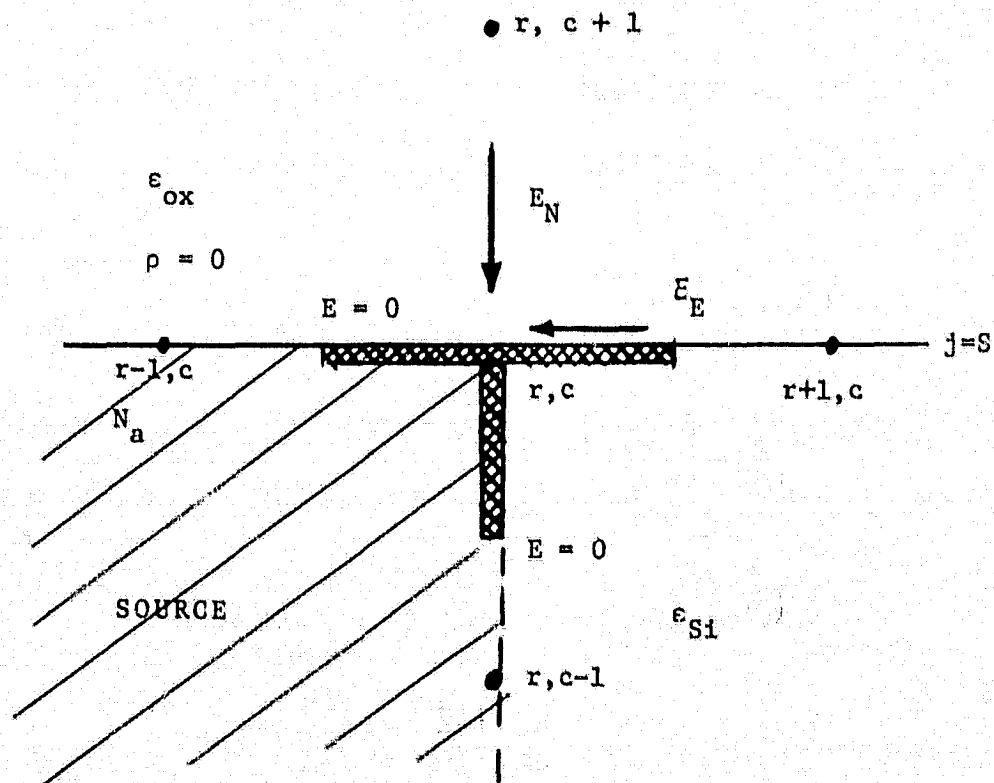


Figure 11. Gauss's law at the source corner

with

$$\rho_{\text{eff}} = - \frac{2q(S + N_a h_{c-1}/2)}{V_T (h_c + h_{c-1})}$$

Therefore, the finite difference form of the equation is obtained by modifying the following terms in equation (18):

$$E = 2 \left(\frac{\epsilon_{\text{ox}}}{\epsilon_{\text{Si}}} \right) [h_c (h_{c-1} + h_c)]^{-1}, \quad (27)$$

$$C = -(A + B + D + E), \quad \text{and}$$

$$\frac{\rho_{\text{eff}}}{\epsilon_{\text{Si}}} = \frac{2q}{V_T \epsilon_{\text{Si}}} \frac{(S + N_a h_{c-1}/2)}{(h_c + h_{c-1})}$$

[Note: $y = J_{\text{max}}$ for the channel node in the program.]

Similarly the linearized version is modified by

$$\bar{E}_i = E_i, \quad \bar{C}_i = C_i, \quad \text{and} \quad (28)$$

$$\begin{aligned} F_{i,c}^r = & A_i U_{i,c-1} + B_i U_{i-1,c} + C_i U_{i,c} \\ & + D_i U_{i+1,c} + E_i U_{i,c+1} + \rho_{\text{eff}}^i / \epsilon_{\text{Si}} \end{aligned}$$

where the subscript i has been inserted to denote the coefficients for mesh node (i,c) .

In the region of $\text{Si} - \text{SiO}_2$ interface where the Q_{ss} charges are assumed to exist, one mesh node is assumed inside the oxide, the coefficients are

$$\bar{A} = A, \quad \bar{B} = B, \quad \bar{C} = C, \quad \bar{D} = D, \quad \bar{E} = E, \quad \text{and}$$

$$F^r = Au_{1,c} + Bu_{i-1,c+1} + Cu_{i,c+1} + Du_{i+1,c+1} + Eu_{i,c+2} + \frac{2Q_{SS}}{\epsilon_{ox} V_T} [h_c + h_{c+1}]^{-1} \quad (29)$$

Similarly, in the oxide where $\rho = 0$, the coefficients are

$$\bar{A} = A, \bar{B} = B, \bar{C} = C, \bar{D} = D, \bar{E} = E, \text{ and} \quad (30)$$

$$F^r = AU_{i,j-1} + BU_{i-1,j} + CU_{i,j} + DU_{i+1,j} + EU_{i,j+1}$$

E. The Channel Conduction Equation, Difference Form

As noted previously, a significant assumption utilized to facilitate convergence, is that the channel charge is modeled as a sheet charge at the silicon-silicon dioxide interface. The channel current is assumed to obey the single dimensional form of the conventional three dimensional equation, i.e.,

$$J_n = q D_n \frac{\partial S}{\partial x} + q \mu_n S E_x \quad (31)$$

where S = density of electrons in channel (#per unit area),
 D_n = electron diffusion constant,
 μ_n = electron mobility, normally field dependent, and
 E_x = tangential electric field component.

The above equation can be written in normalized form utilizing

$$E_x = V_T \frac{\partial U}{\partial x} \text{ and } D_n = V_T \mu_n \text{ (Einstein's relationship):}$$

$$J_n = q V_T \mu_n \left(\frac{\partial S}{\partial x} - S \frac{\partial U}{\partial x} \right) \quad (32)$$

$$\text{Then} \quad f_S = (S - U' S) \mu_n \quad (33)$$

$$\text{where } f_S = J_n (q V_T)^{-1}, \quad S' = \frac{\partial S}{\partial x}, \quad \text{and } U' = \frac{\partial U}{\partial x}.$$

At any point x in the channel the general solution of S is

$$S(x) = \exp \int_{x_{i-1}}^x U' dx \left\{ \int_{x_{i-1}}^x \left(\frac{f_S}{\mu_n} \exp \int_{x_{i-1}}^x U' dx \right) dx + C \right\} \quad (34)$$

which reduces to the specific solution for $S(x)$, given

$$S \text{ at } x = x_{i-1} : \\ S(x) e^{-U} = S_{i-1} e^{-U_{i-1}} + \frac{J_n}{q V_T} \int_{x_{i-1}}^x \frac{e^{-u(\xi)}}{\mu(\xi)} d\xi \quad (35)$$

Rewriting the above leads to S_i in terms of S_{i-1} :

$$\frac{S_i \exp(-U_i) - S_{i-1} \exp(-U_{i-1})}{\int_{x_{i-1}}^{x_i} \frac{\exp[-U(\xi)] d\xi}{\mu(\xi)}} = \frac{J_n}{q V_T} \quad (36)$$

Similarly, integrating between x_i and x_{i+1} leads to

$$\frac{S_{i+1} \exp(-U_{i+1}) - S_i \exp(-U_i)}{\int_{x_i}^{x_{i+1}} \frac{\exp[-U(\xi)] d\xi}{\mu(\xi)}} = \frac{J_n}{q V_T} \quad (37)$$

Assuming current continuity, i.e., $J_n = \text{constant}$, leads to

$$\begin{aligned}
& - \left\{ \exp - (U_{i-1}) \int_{x_i}^{x_{i+1}} \frac{\exp - U(\xi)}{\mu(\xi)} d\xi \right\} S_{i-1} \\
& + \left\{ \exp - U_i \int_{x_{i-1}}^{x_{i+1}} \frac{\exp (U(\xi))}{\mu(\xi)} d\xi \right\} S_i \\
& - \left\{ \exp - U_{i+1} \int_{x_{i-1}}^{x_i} \frac{\exp (-U(\xi))}{\mu(\xi)} d\xi \right\} S_{i+1} = 0 .
\end{aligned} \tag{38}$$

The above equation is of the form

$$a_i S_{i-1} + b_i S_i + c_i S_{i+1} = 0$$

and define a tridiagonal linear system of equations.

Equation 36 should reduce to a familiar form as $x_i - x_{i-1} = \Delta x \rightarrow 0$.

Let $S_{i-1} = S_o$, $S_i = S_o + \Delta S$, $U_{i-1} = U_o$, $U_i = U_o + \Delta U$. Then 36 becomes

$$\frac{(S_o + \Delta S) e^{-U_o} (1 - \Delta U) - S_o e^{-U_o}}{\mu^{-1} e^{-U_o} \Delta x} = \frac{J_n}{qV_T} \tag{39}$$

which reduces to

$$J_n = qV_T \mu \left\{ \frac{\Delta S}{\Delta x} - S_o \frac{\Delta U}{\Delta x} \right\} \tag{40}$$

which displays the familiar diffusion and drift terms in the limit.

The integral form in (36) has the potential of being more accurate with larger grid spacing.

Another observation one may note is that the coefficients a_i , b_i , c_i may be scaled, or normalized, to values less dependent

on the exponential of potential by multiplying them by $\exp(2U_1)$ which gives

$$\begin{aligned} a_1 &= - \exp(U_1 - U_{i-1}) \int_{x_1}^{x_{i+1}} \mu(\xi) \exp[U_1 - U(\xi)] d\xi, \\ b_1 &= \int_{x_{i-1}}^{x_{i+1}} \mu^{-1}(\xi) \exp[U_1 - U(\xi)] d\xi, \quad \text{and} \\ c_1 &= \exp(U_1 - U_{i+1}) \int_{x_{i-1}}^{x_1} \mu^{-1}(\xi) \exp[U_1 - U(\xi)] d\xi. \quad (41) \end{aligned}$$

And, of course, if the mobility is assumed constant, then it can be removed by multiplying through by μ .

Noting that the integrand varies exponentially with potential whereas the potential is expected to vary with x no worse than the third power, one can approximate the integral by assuming

$$U - U_0 = a(x - x_0) \quad (42)$$

and evaluate the slope $a = \frac{dU}{dx}$ at the lowest value of potential over the range of integration. In this manner the neglected higher order terms contribute very little error since the integrand falls off exponentially with potential. Changing variables for the integration of b_1 , as an example, leads to

$$b_1 = \int_{U_{i-1}}^{U_{i+1}} \frac{\mu^{-1}(U)}{a} \exp[U_1 - U] dU \quad (43)$$

where

$$a = \frac{dU}{dx}. \quad \text{Further,}$$

$$b_1 = [a\mu]^{-1} \{ \exp(U_1 - U_{i-1}) - \exp(U_1 - U_{i+1}) \} \quad (44)$$

with a and μ evaluated at the lowest value of U which for $a > 0$ is U_{i-1} . Similarly,

$$\begin{aligned} a_1 &= [a\mu]_i^{-1} [\exp(U_i - U_{i+1}) - 1] \exp(U_i - U_{i-1}) \\ c_1 &= [a\mu]_{i-1}^{-1} [1 - \exp(U_i - U_{i-1})] \exp(U_i - U_{i+1}) \\ b_1 &= [a\mu]_{i-1}^{-1} [\exp(U_i - U_{i-1}) - \exp(U_i - U_{i+1})] \end{aligned} \quad (45)$$

where the subscript on $[a\mu]$ denotes the node for evaluating a and μ , assuming $a > 0$.

The boundary conditions for this system of equations association with electron conduction in the channel must be defined in terms of the source and drain corner mesh nodes for the MOSFET operation in the active region. Figure 11 illustrates the application of Gauss's Law at the source corner of the channel. Mesh nodes along the boundary of the source are common potential, therefore, the tangential electric field terms along the boundary of the source are zero. Since the electric field along the channel E_E for operations of interest - at least at this source corner, the surface charge is modelled in a single dimensional manner, i.e.,

$$\epsilon_{ox} E_N = -qS \quad (46)$$

or, in terms of potential,

$$\frac{V_T \epsilon_{ox} (U_{r,c+1} - U_{r,c})}{h_c} = qS \quad (47)$$

An alternate scheme involves the solution of the one dimensional Poisson equation:

$$- \frac{\epsilon_{ox}}{f_{ox}} \left\{ (V_G - \phi_{ms}) - (V_C + V_{Bi}) \right\} = Q_{ss} - qS + Q_B \quad (48)$$

where V_G = the applied bias to the gate

ϕ_{ms} = the gate work function relative to the substrate,

V_C = the applied channel potential,

V_{Bi} = the work function of the drain/source,

t_{ox} = oxide thickness,

ϵ_{ox} = oxide permittivity,

Q_{ss} = silicon dioxide-silicon interface charge,

q = electronic charge, and

Q_B = the bulk charge density (per unit area)

= 0 for drain and source.

The Q_B expression can be defined in terms of the vertical electric field in the channel region:

$$Q_B = \epsilon V_T \frac{(U_{c-1} - U_c)}{h_{c-1}} - q N_a \frac{h_{c-1}}{2}$$

where the subscript c refers to the channel node.

F. Channel Coupled Equations

Although the channel conduction equation (38) is linear in S , it is nonlinear in potential. The simultaneous solution of the conduction equation and the Poisson equation along the channel

requires linearizing (38).

Let $F_{ci}^r = a_i S_{i-1} + b_i S_i + c_i S_{i+1}$ where a_i, b_i, c_i are defined in (45). Since the terms $[a\mu]^{-1}$ vary more slowly than the exponential terms, the term is assumed constant for any particular iteration, using the last known values of u 's for its evaluation. Then, the linearized conduction equation becomes

$$\begin{aligned} A_{ci} &= \frac{\partial F_{ci}^r}{\partial U_{i-1}} = -a_i S_{i-1} [a\mu]_{i-1}^{-1} S_i \exp(U_i - U_{i-1}) \\ &\quad + c_i S_{i+1} \exp(U_i - U_{i-1}) [1 - \exp(U_i - U_{i-1})]^{-1}, \\ B_{ci} &= a_i, \\ C_{ci} &= \frac{\partial F_{ci}^r}{\partial U_i} = -a_i S_{i-1} [\exp(U_i - U_{i+1}) - 1]^{-1} + b_i S_i \\ &\quad + c_i S_{i+1} [1 - \exp(U_i - U_{i-1})]^{-1} [1 - 2 \exp(U_i - U_{i-1})], \\ D_{ci} &= b_i, \\ E_{ci} &= \frac{\partial F_{ci}^r}{\partial U_{i+1}} = -a_i S_{i-1} \exp(U_i - U_{i+1}) [\exp(U_i - U_{i-1}) - 1]^{-1} \\ &\quad + b_i S_i \exp(U_i - U_{i+1}) [\exp(U_i - U_{i-1}) - \exp(U_i - U_{i+1})]^{-1} \\ &\quad - c_i S_{i+1}, \\ G_{ci} &= c_i, \text{ and} \\ F_{ci}^{r+1} &= F_{ci}^r + A_{ci} \Delta U_{i-1} + B_{ci} \Delta S_{i-1} + C_{ci} \Delta U_i + D_{ci} \Delta S_i \quad (49) \\ &\quad + E_{ci} \Delta U_{i+1} + G_{ci} \Delta S_{i+1} = 0. \end{aligned}$$

The Poisson equation has been previously derived, equations (27) and (28), with the coefficients being defined below for the new system of equations:

$$\begin{aligned} & \bar{B}_1 \Delta U_{i-1,c} + \bar{C}_1 \Delta U_{ic} + \bar{H}_1 \Delta S_1 + D_1 \Delta U_{i+1,c} \\ & = -\bar{A}_1 \Delta U_{i,c-1} - \bar{E}_1 \Delta U_{i,c+1} - F_{1,c}^r = T_{1c}^r \end{aligned} \quad (50)$$

where

$$\bar{H}_1 = -2q[\epsilon_{si} V_T (h_{1,c} + h_{1,c-1})]^{-1},$$

$$\bar{A}_1 = A_1 \text{ from (17) ,}$$

$$\bar{B}_1 = B_1 \text{ from (17) ,}$$

$$\bar{D}_1 = D_1 \text{ from (17) ,}$$

$$\bar{E}_1 = E_1 \text{ from (17) ,}$$

$$C_1 = C_1 \text{ from (17) ,}$$

$$F_{1,c}^r = \text{as defined in (28) .}$$

Simultaneously solving for the channel potential and the change charge requires the simultaneous solution of the above two equations (49) and (50) which results in the following system of equation in matrix form:

$$\begin{bmatrix} \bar{C} & \bar{H} & \bar{D} & 0 & 0 & 0 & . & . & . & . & . \\ C & D & E & G & 0 & 0 & . & . & . & . & . \\ \bar{B} & 0 & \bar{C} & \bar{H} & \bar{D} & 0 & . & . & . & . & . \\ A & B & C & D & E & G & 0 & . & . & . & . \\ 0 & 0 & \bar{B} & 0 & \bar{C} & \bar{H} & \bar{D} & 0 & . & . & . \\ 0 & 0 & A & B & C & D & E & G & 0 & . & . \\ & & / & / & / & / & / & / & & & \end{bmatrix} \begin{bmatrix} \Delta U_2 \\ \Delta S_2 \\ \Delta U_3 \\ \Delta S_3 \\ . \\ . \\ . \\ \Delta U_{N-1} \\ \Delta S_{N-1} \end{bmatrix} = \begin{bmatrix} T_{2c} \\ -F_{2c} \\ T_{3c} \\ -F_{3c} \\ . \\ . \\ . \\ T_{N-1,c} \\ -F_{N-1,c} \end{bmatrix}$$

The matrix is a 6 diagonal matrix. The number of variables is twice the number of grid points within the channel--not counting the boundary nodes at the source or drain. The solution can be conveniently solved by using a Gaussian elimination technique.

G. Overall Flow Chart

In order to expedite convergence, initially, the gradual channel approximation is assumed and the potential is calculated along the channel. This analytical approach divides the device cross-section into two regions, the channel, silicon substrate region and the oxide region.

In each of the two regions an initial approximation of the potential distribution is obtained by solving the one-dimensional form of Poisson's equation utilizing the given boundary potentials including the channel potential derived in the previous step. The one-dimensional equation is equivalent to setting $dU/dx = 0$. The potential distribution is found along one column (vertical) simultaneously. By sweeping in the x direction, i.e., repeat the solution on another column, the potential distribution for the entire region(s) is obtained.

Next the solution to the two dimensional P. E. is obtained in each region. In the oxide the potential along a column is obtained with the region being swept in the x-direction. In the silicon convergence is expedited by using the alternating direction implicit (ADI) scheme. First, the potential in the row below the channel (JMAX0) is obtained. Next the potential distributions for

each row between the source and drain are obtained by sweeping in the negative y-direction. When the solution to row JKL is obtained, the solution to the column $I = 1$ is obtained. The column solutions are obtained by sweeping in the positive x-direction. This ADI scheme is repeated until satisfactory convergence is obtained.

With the two-dimensional potential distribution obtained for both regions based on the gradual channel assumption, a new estimate of the channel potential and the channel charge is obtained by solving simultaneously the P. E. and current equation along the channel row. The 2-D P. E. is then solved along the rows between the source and drain by sweeping y in the negative direction. Next the columns solutions are obtained sweeping the x-direction for the entire regions--thus crossing the channel in the appropriate locations ($I = I_K + 1$ to $I_L - 1$). This ADI scheme starting at the simultaneous solution of the P. E. and the current equation along the channel row is repeated until satisfactory convergence is obtained.

The channel current is obtained from an explicit solution to the channel current equation after the channel charge and potential are found.

H. Progress Report

The basic program has been written which provides user flexibility for defining the physical dimensions, the number of grid points, p or n type device, metal or silicon gate, type orientation of substrate, etc. Provisions have been incorporated

for sweeping multiple bias points in order to plot, for example, drain or transfer characteristics. In addition, provisions are provided to plot the two dimension potential distribution as well as, print out this data in table form.

Using an example bias the program has successfully completed the steps through the solution of the two dimensional P. E. using the fixed channel potential as a boundary condition. However, at the next step, the channel charge is found to diverge. Time has not allowed the resolution of the problem; however, an error has been found in the current equation program which may be the cause. Of deeper concern is the possibility that the channel charge is not directly tied to the channel potential through the P. E., but only indirectly. This may require the formulation of an expression for channel charge q_s as a function of potential and electric field which is then inserted into the Poisson equation. Further investigation of this problem is required before the best solution can be determined.

I. Availability of 2-D MOSFET Simulators

The first 2-D simulator program which could provide I-V characteristics was developed by Mock [3.9] and Kennedy [3.8] at IBM in the 1970 to 1972 timeframe. The program, based on finite difference techniques, is proprietary to IBM. However, a modified version of this program has been developed by Sutherland [3.14] (and Kennedy) at the University of Florida under contract to ARPA. This program is restricted to uniformly doped substrates and zero

substrate bias.

Kennedy at the Applied Electronics Research Corporation has modified the Sutherland program to include provisions for

- 1) 1-D substrate impurity profile,
- 2) mobility dependence on gate voltage, and
- 3) substrate bias

and is now licensing the program (NEMOS) for \$10,000 for one year and \$7,500 for each succeeding year.

In addition, Hitachi has developed a finite element version with provisions, at least, for substrates with 1-D impurity profiles. Dr. Asai of Hitachi has indicated the possibility of licensing the program to Universities, government and industry in the United States. The Hitachi program called CADDET was developed in 1977-1978.

At least one other 2-D simulation program is under development. Jim Meindl at Stanford is under contract with ARPA to continue the work by Sutherland.

At this writing the author has been unable to determine when the program under development at Stanford will be available for distribution.

J. Recommendations

In view of the recent "availability" of alternate sources of the 2-D simulator, it seems prudent to evaluate more seriously the availability and cost for achieving a satisfactory and working program from the four possible sources. The compatibility with existing computers and the difficulty in modifying them to meet

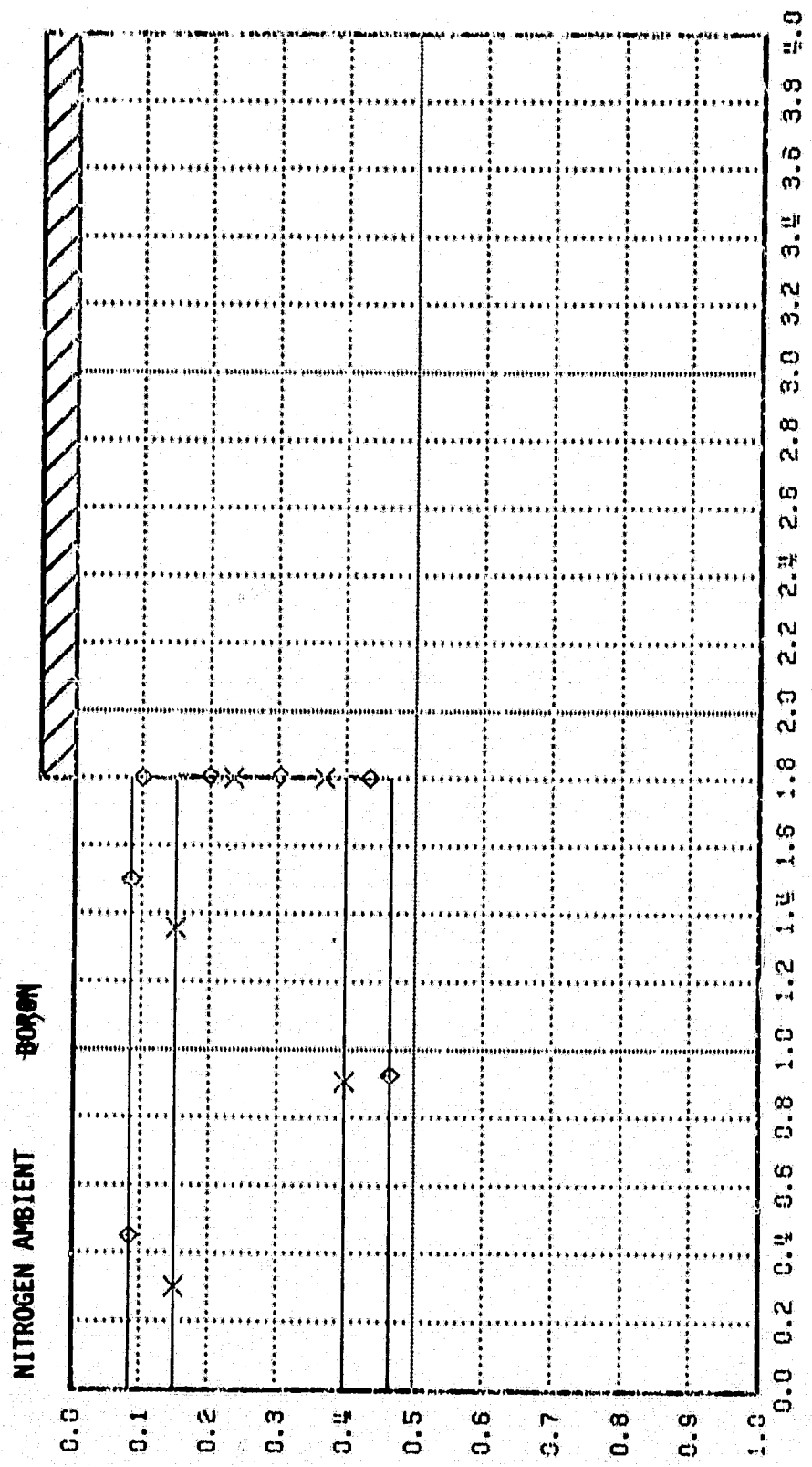
the stated objectives must be considered. The authors believe this should be accomplished before seriously continuing with the present program. After all, the 2-D MOSFET simulator is just the means with which to evaluate various short channel MOSFET device structures and not the end product.

APPENDIX A

BORON DATA

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 TIME = 0.00

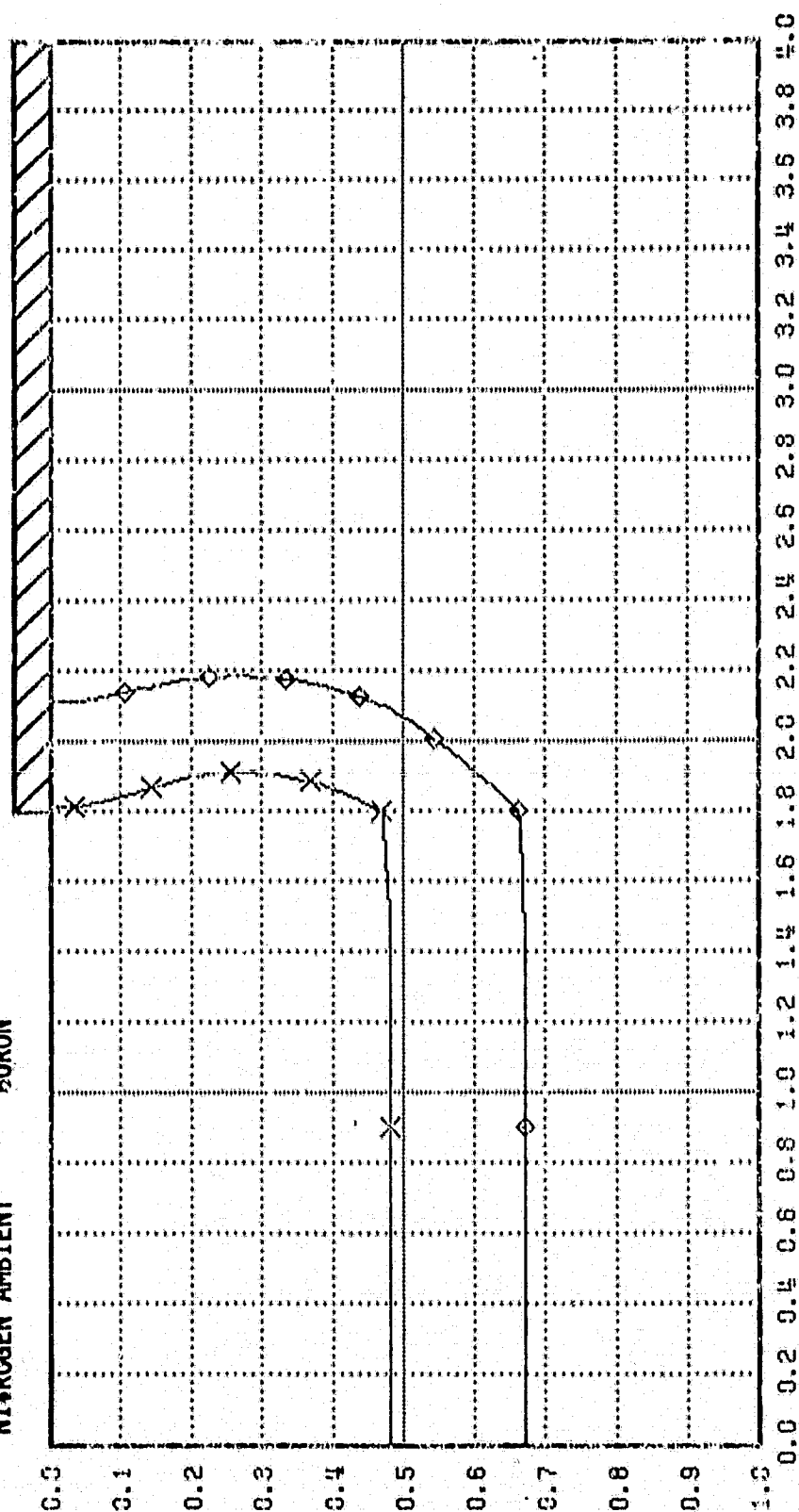
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 □ - 1.0E19
 △ - 1.0E18
 + - 1.0E17
 X - 1.0E16
 ◇ - 1.0E15



λ^2
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 TIME STEP = 1000.
 TIME = 10
 = 0.20

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 O - 1.0E19
 A - 1.0E18
 + - 1.0E17
 X - 1.0E16
 D - 1.0E15

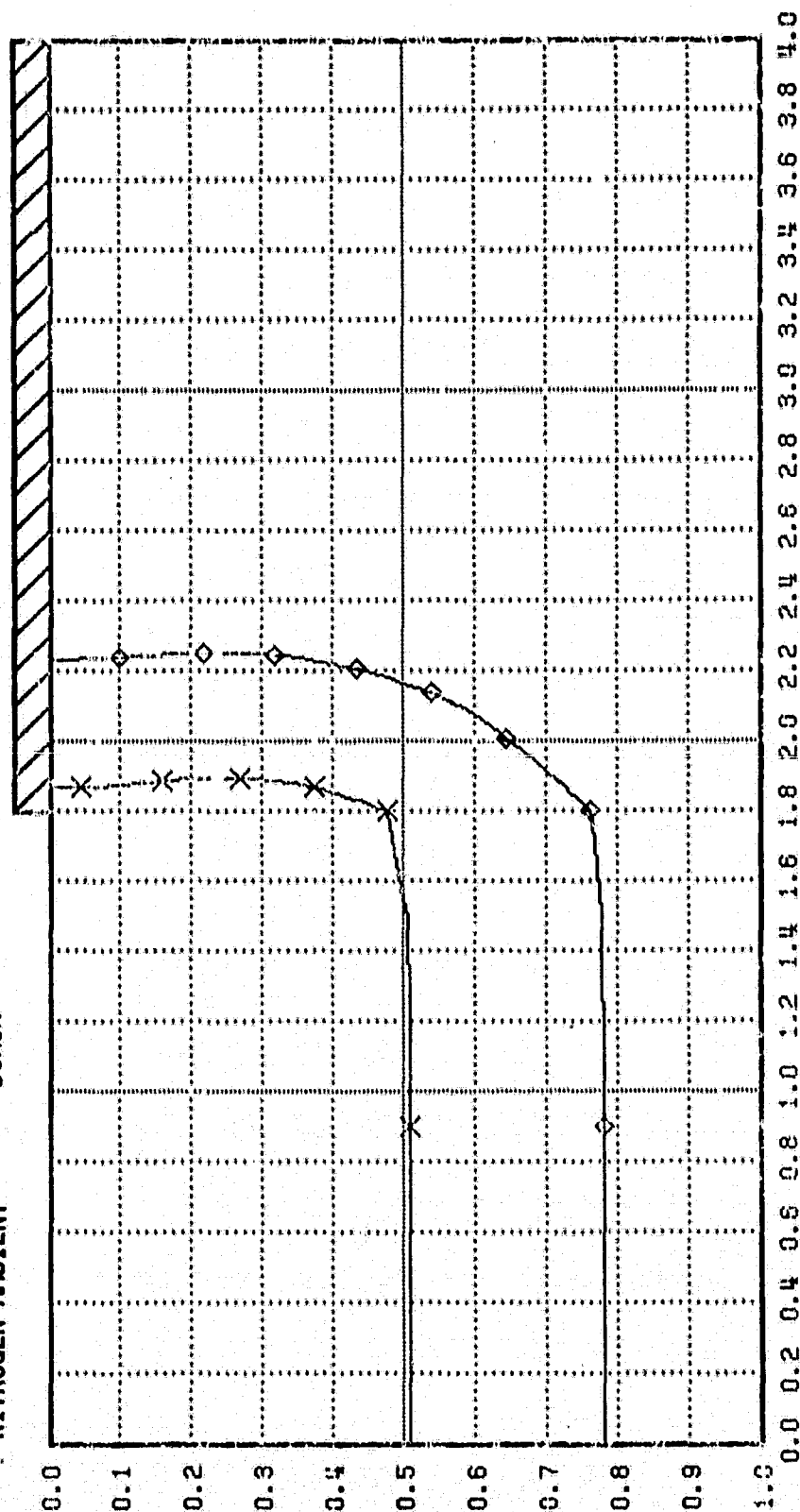
NITROGEN AMBIENT BORON



- 1.0E20
 - 1.0E19
 - 1.0E18
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 - 1.0E16
 - 1.0E15

χ^2
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 = 0.40

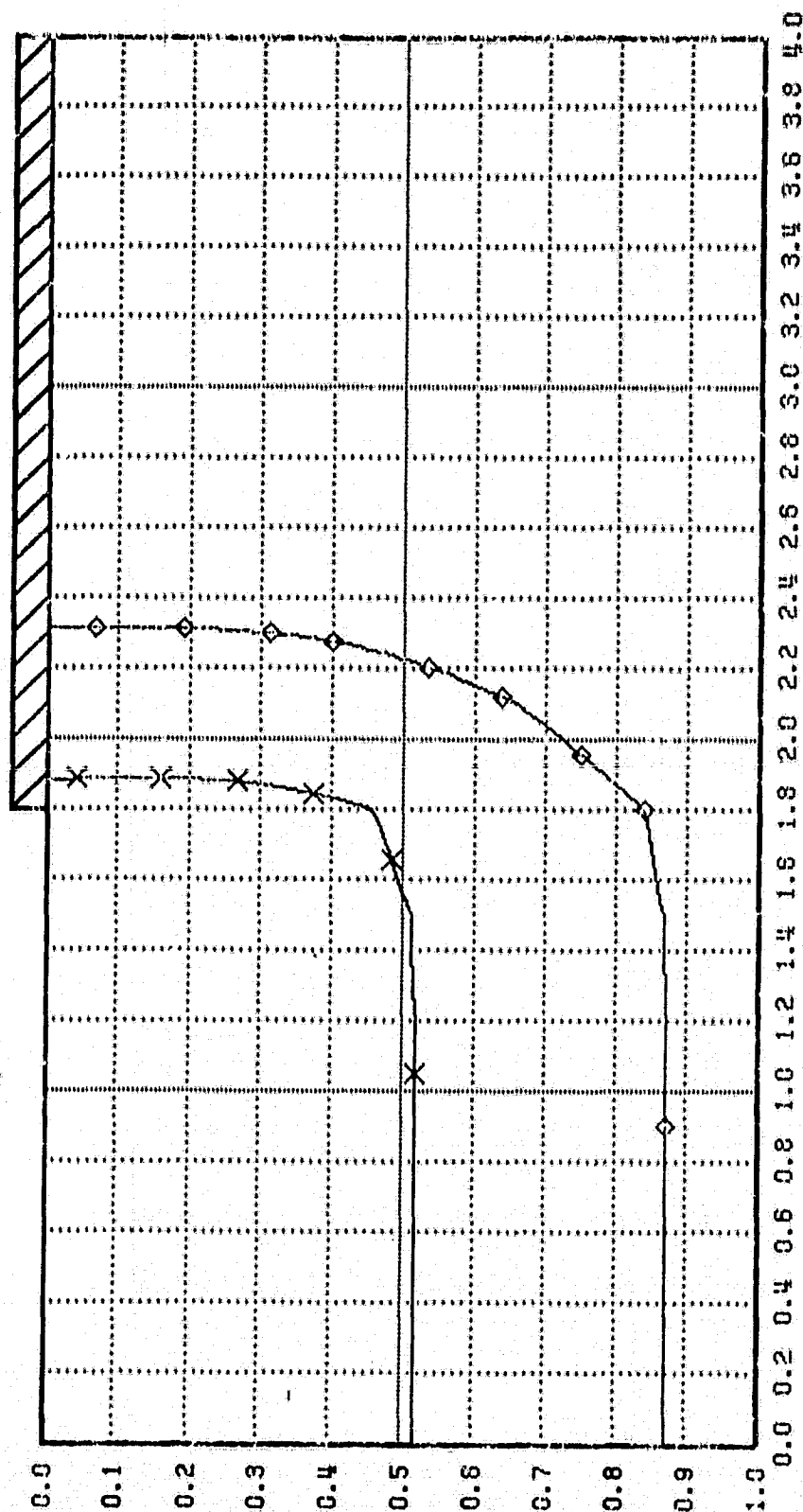
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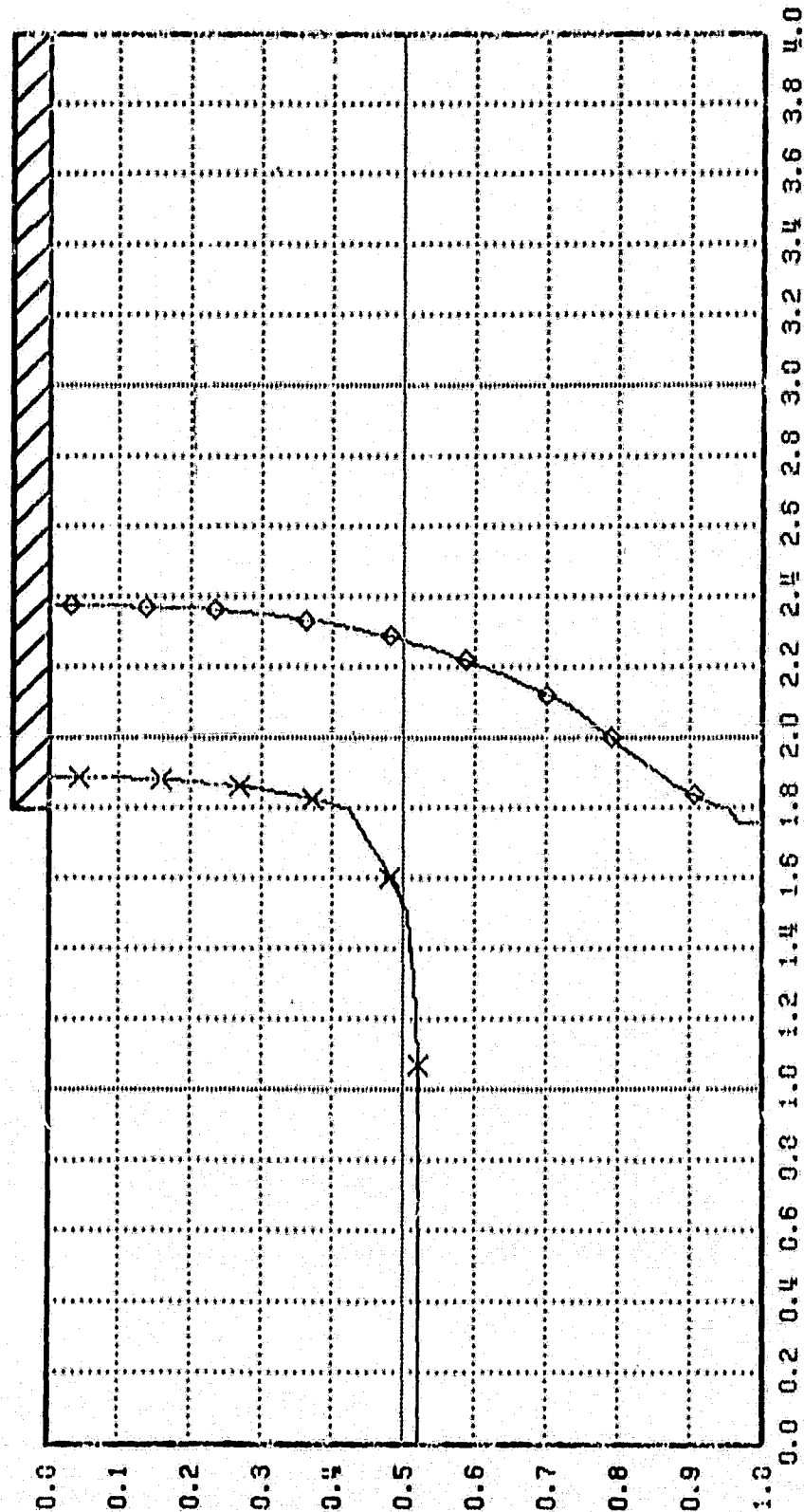
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 TIME = 30
 = 0.60

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 A - 1.0E18
 + - 1.0E17
 X - 1.0E16
 D - 1.0E15

NITROGEN AMBIENT BORON



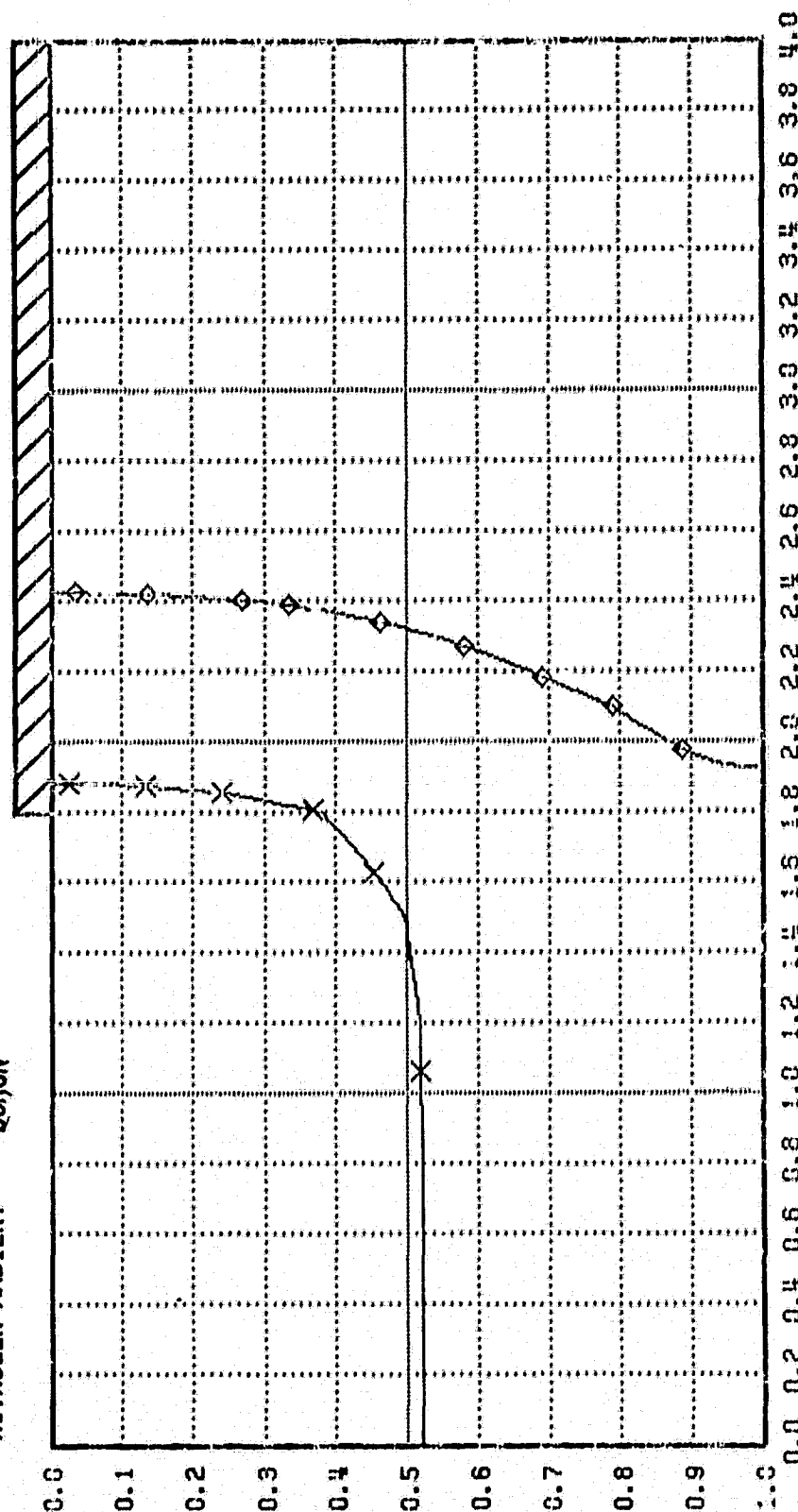
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 BORON

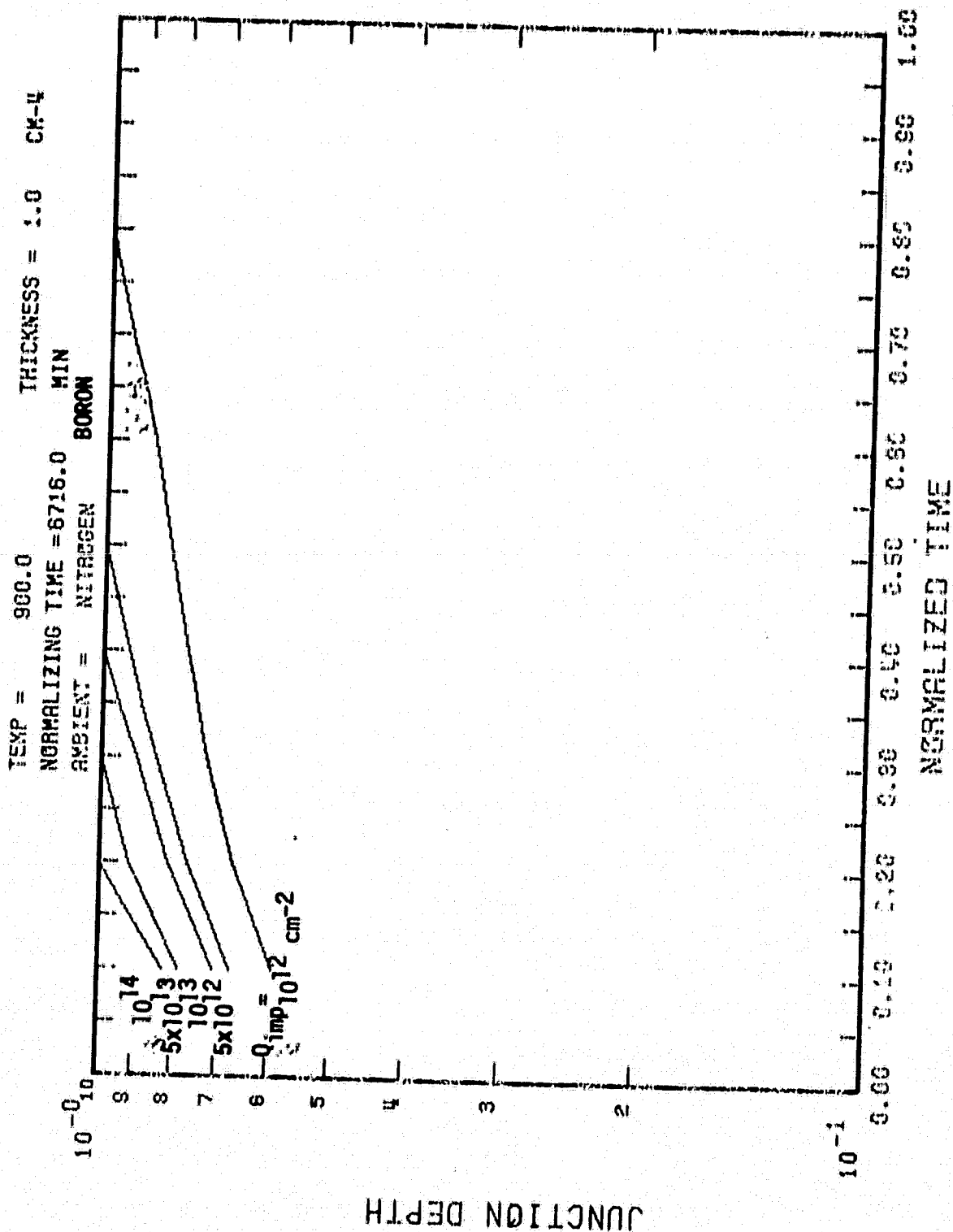


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 - 1.0E18
 - 1.0E17
 - 1.0E16
 - 1.0E15

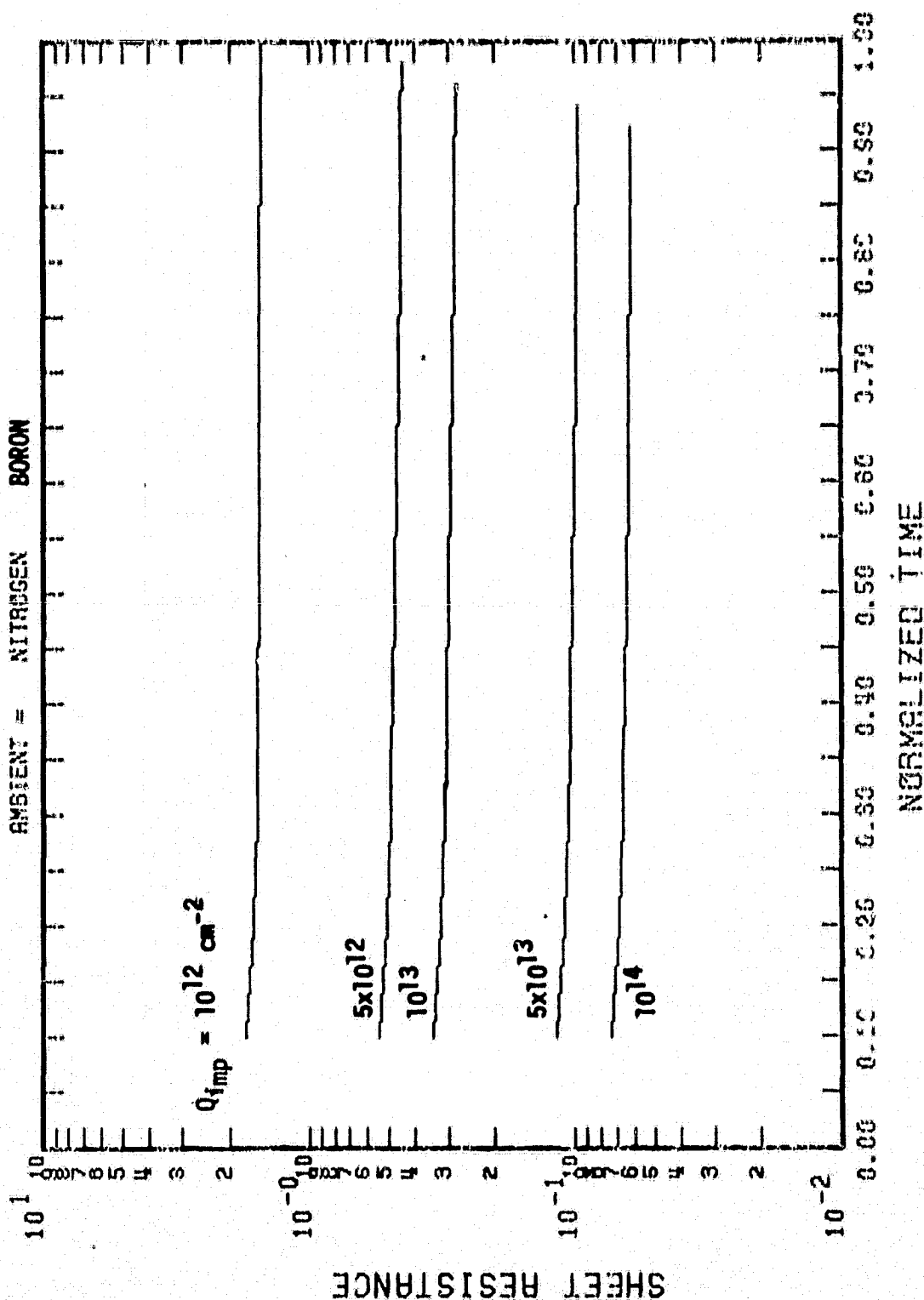
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 = 1.00

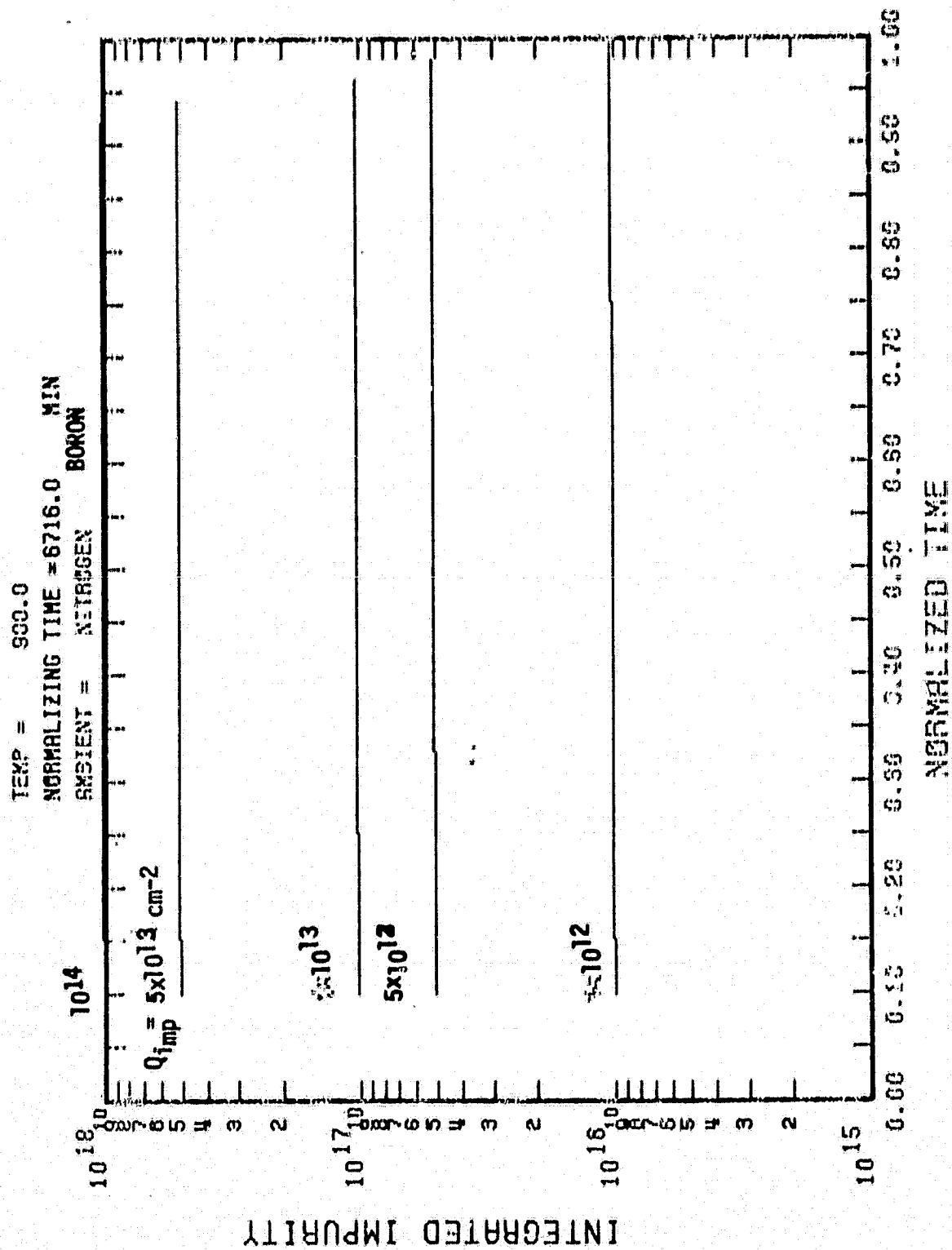
NITROGEN AMBIENT REGION

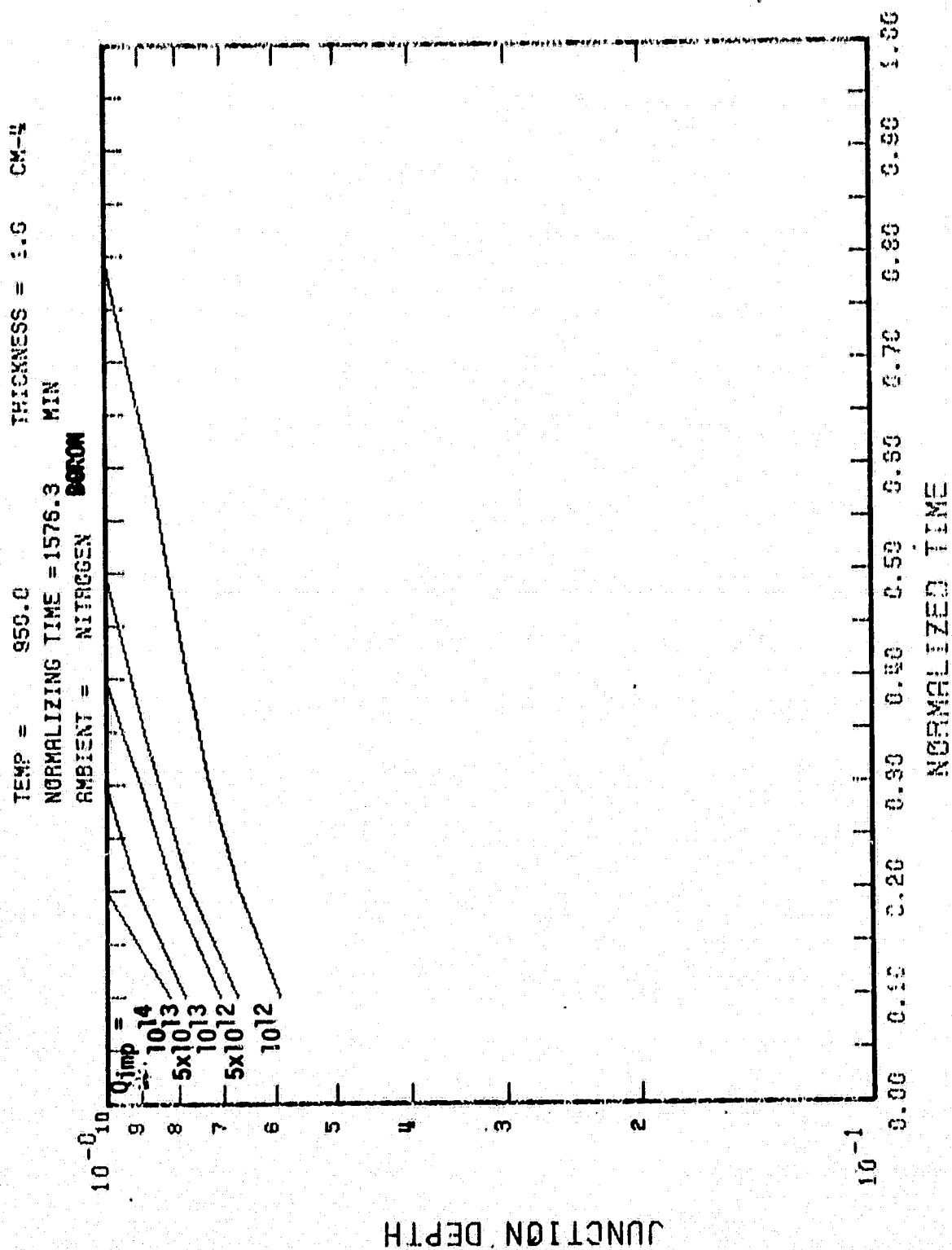




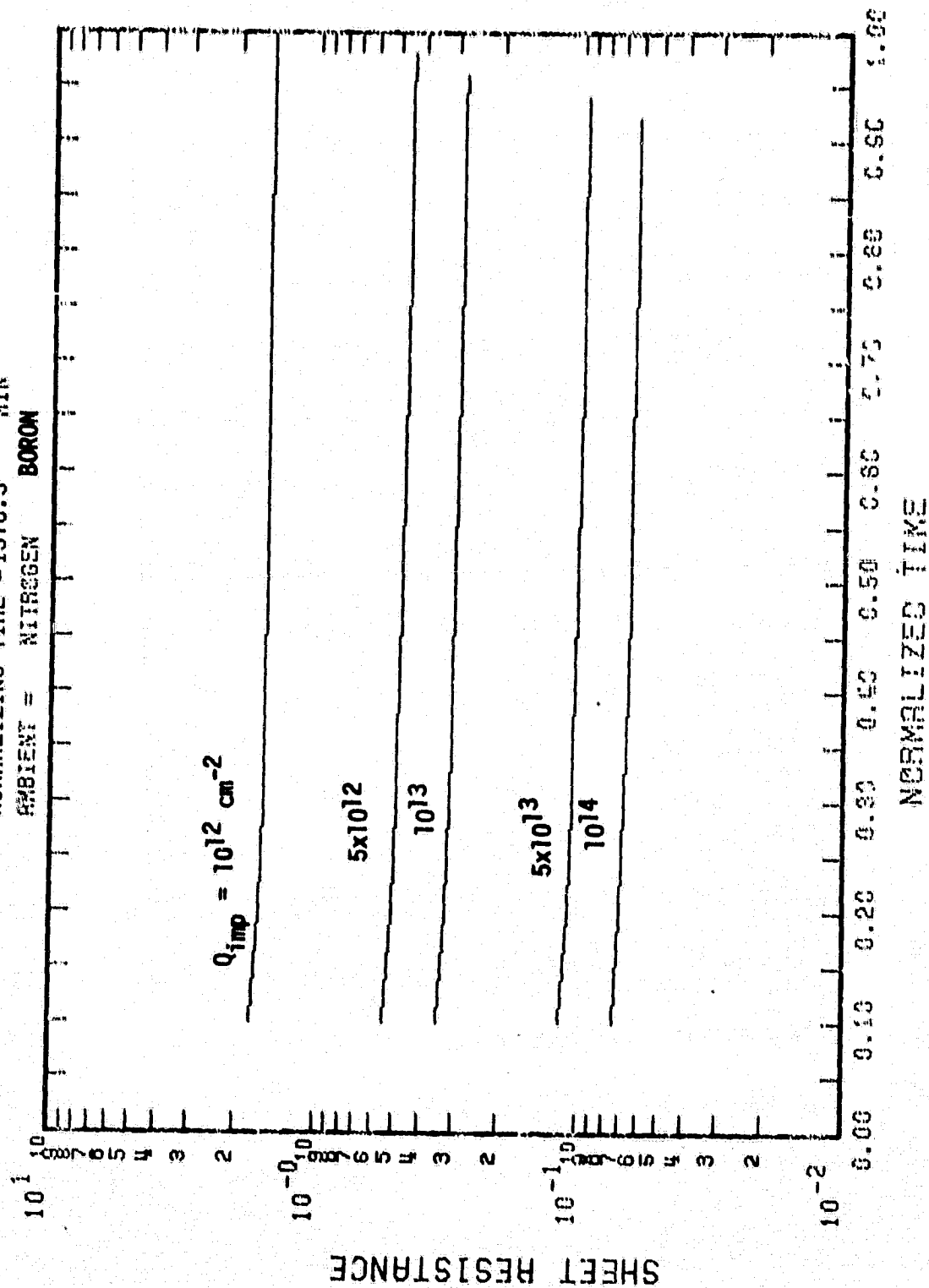
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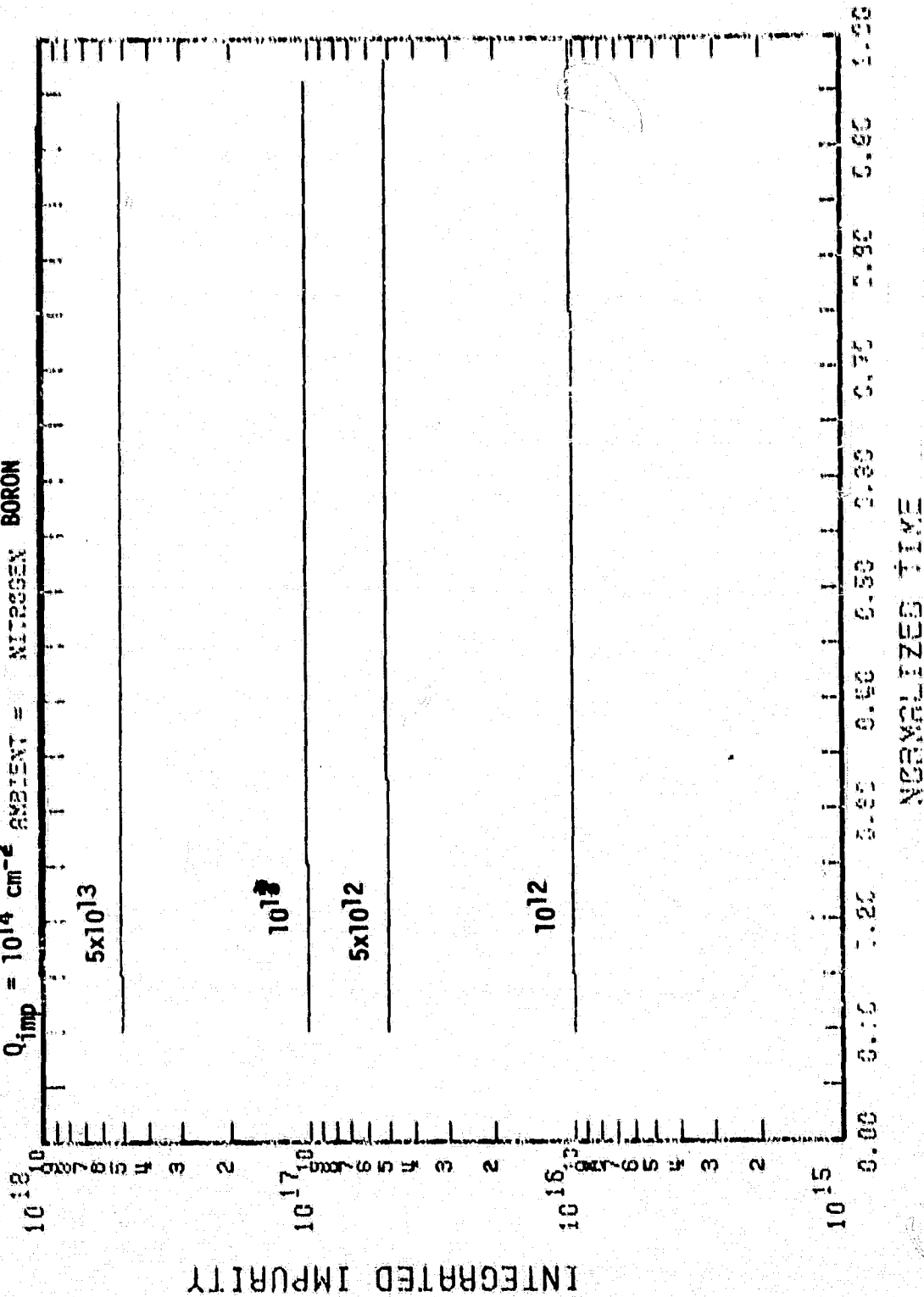


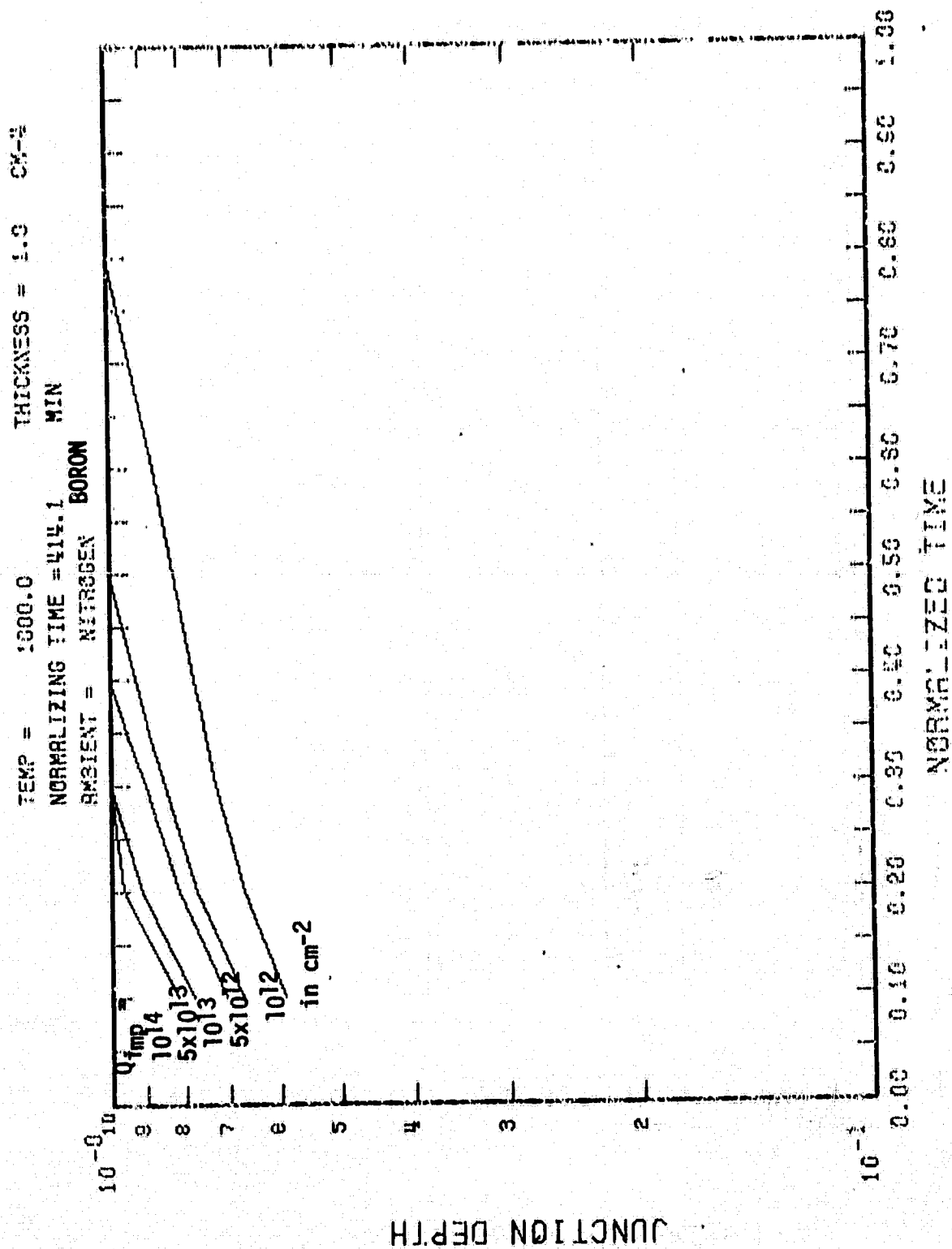


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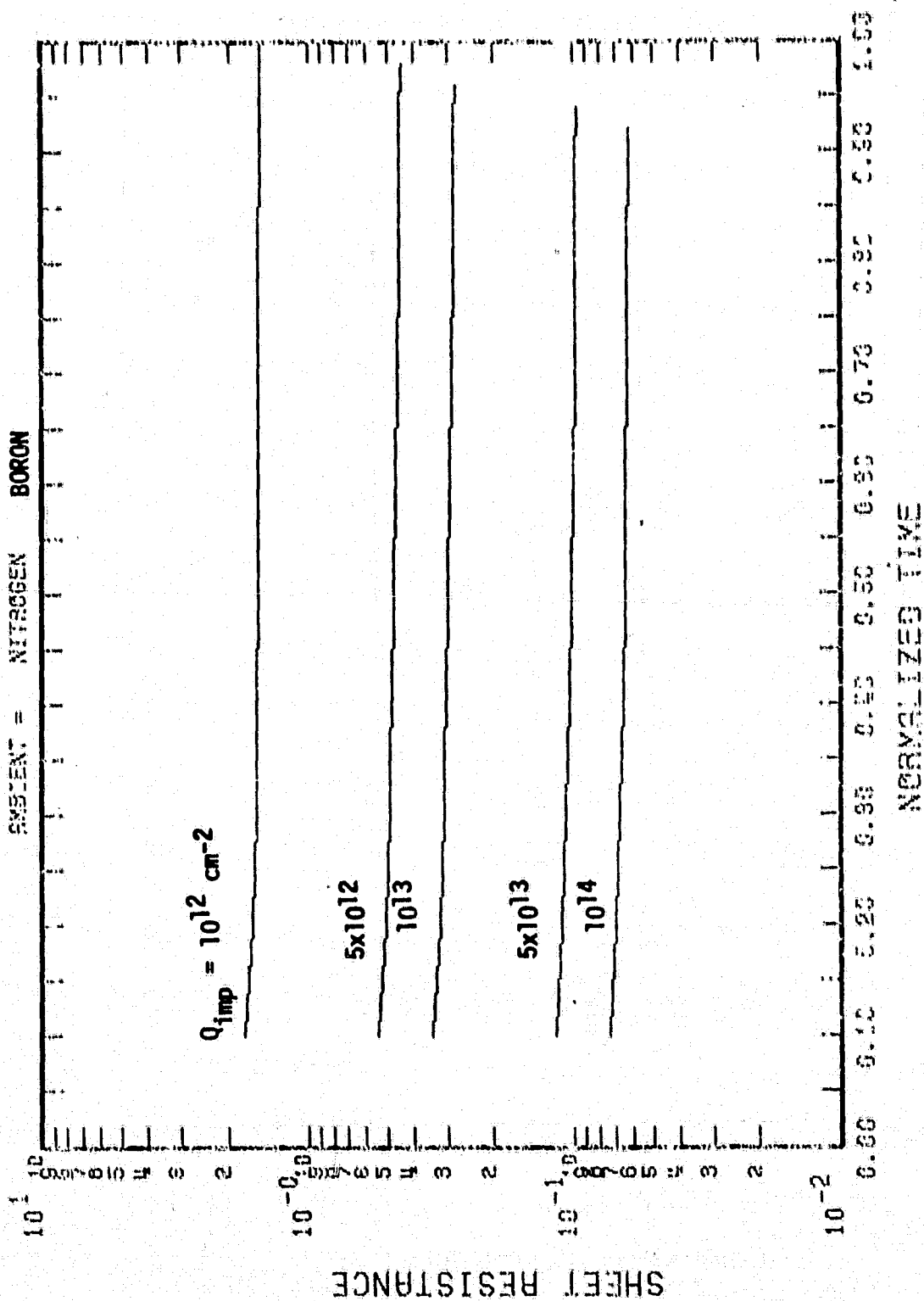
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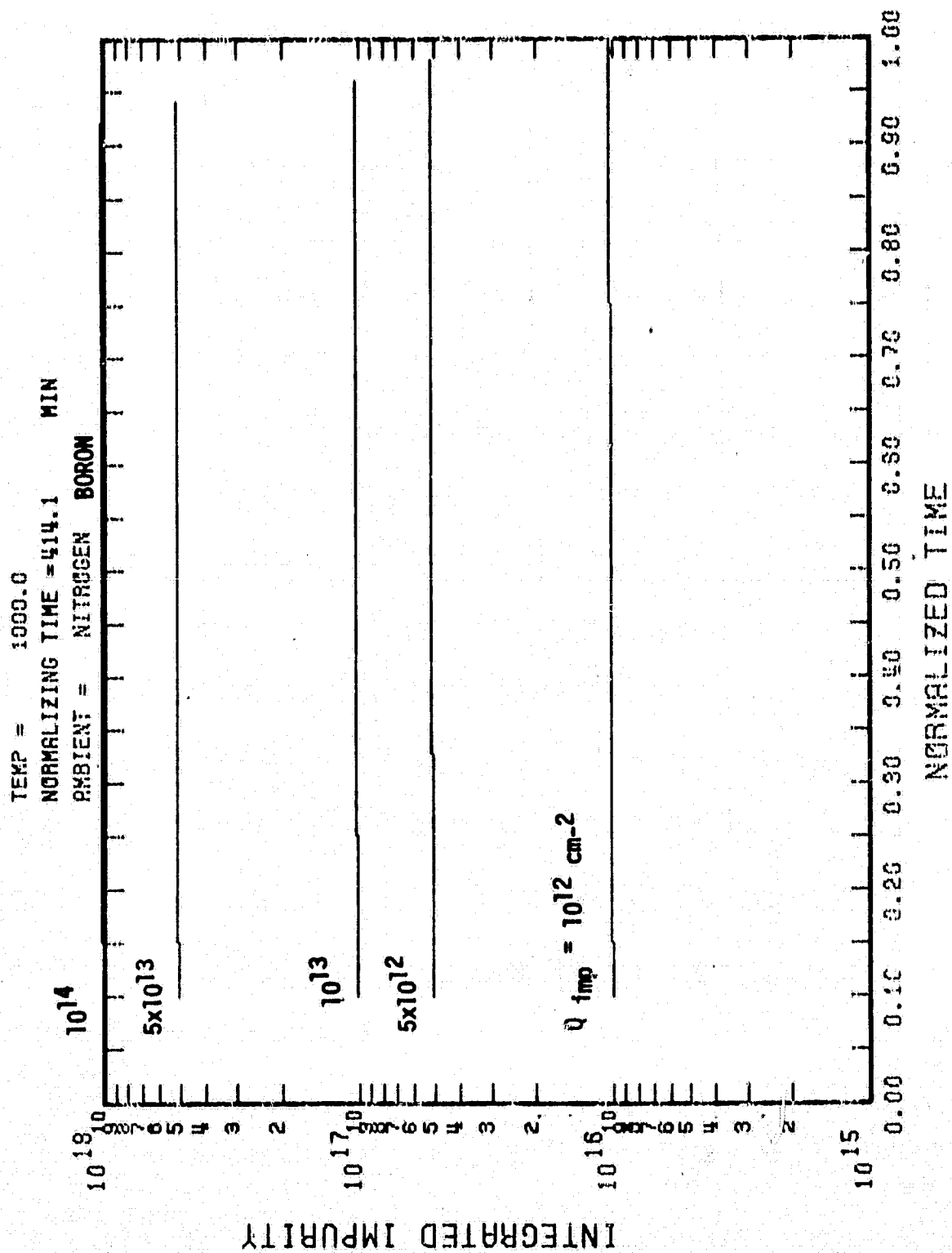




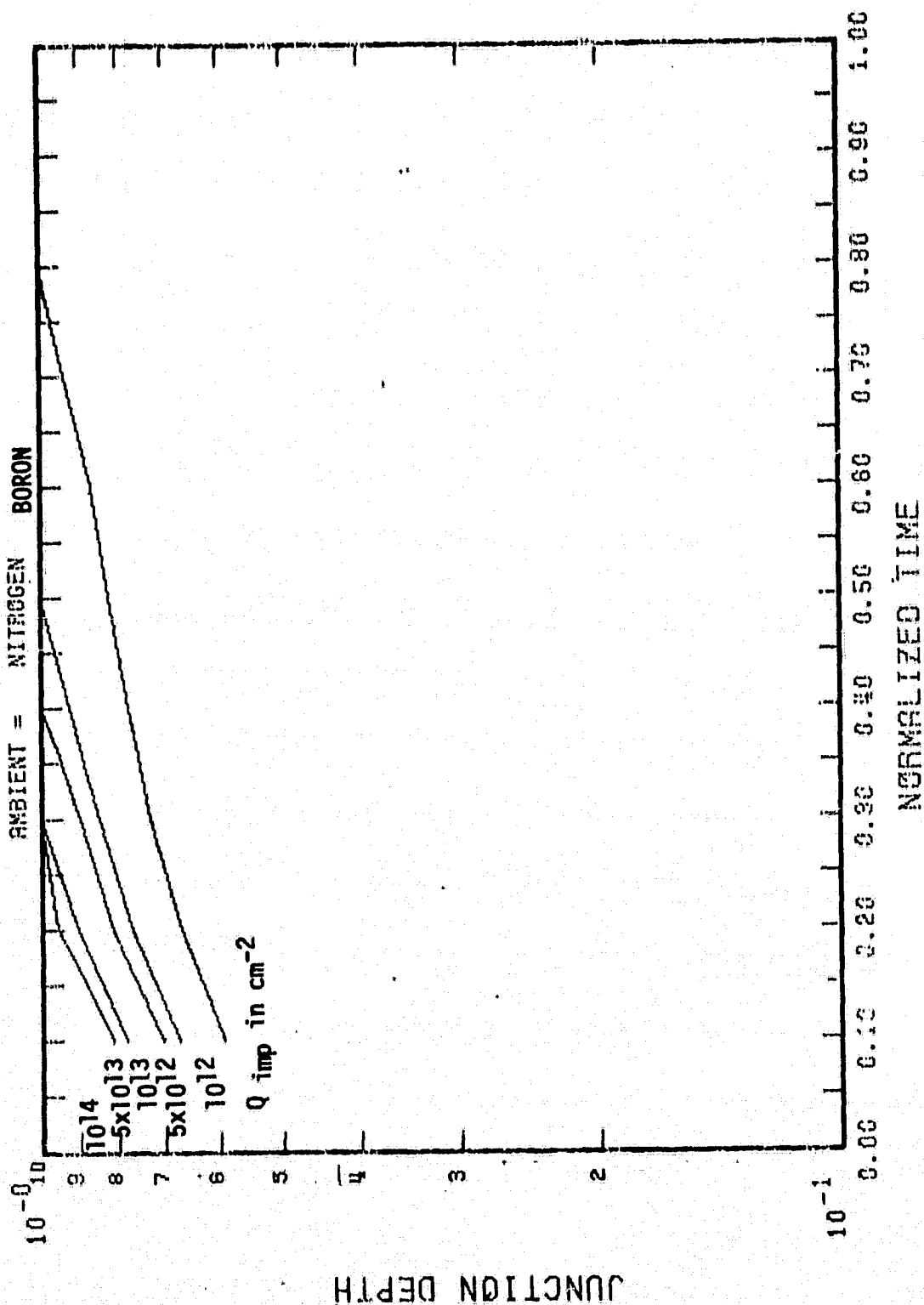
JUNCTION DEPTH

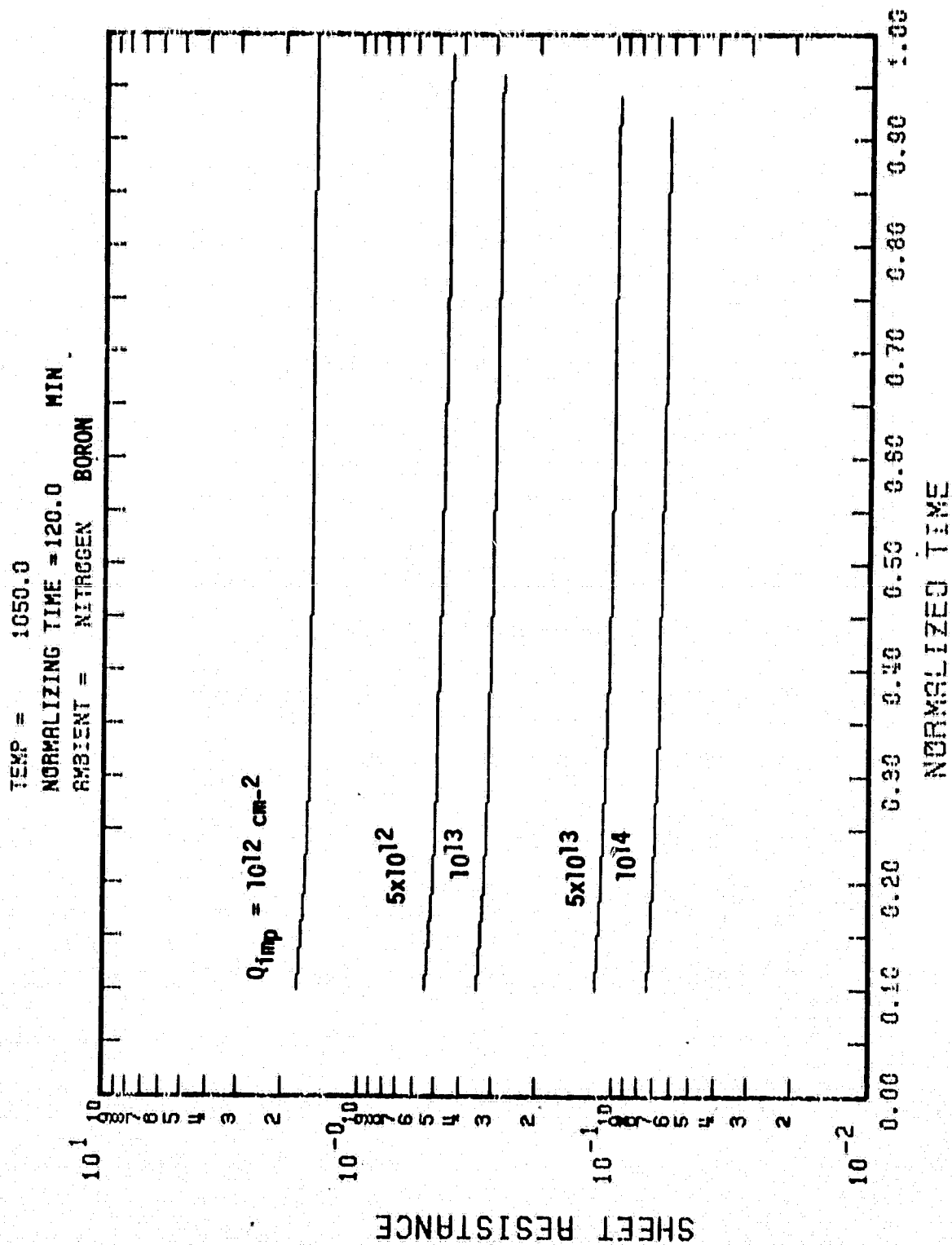
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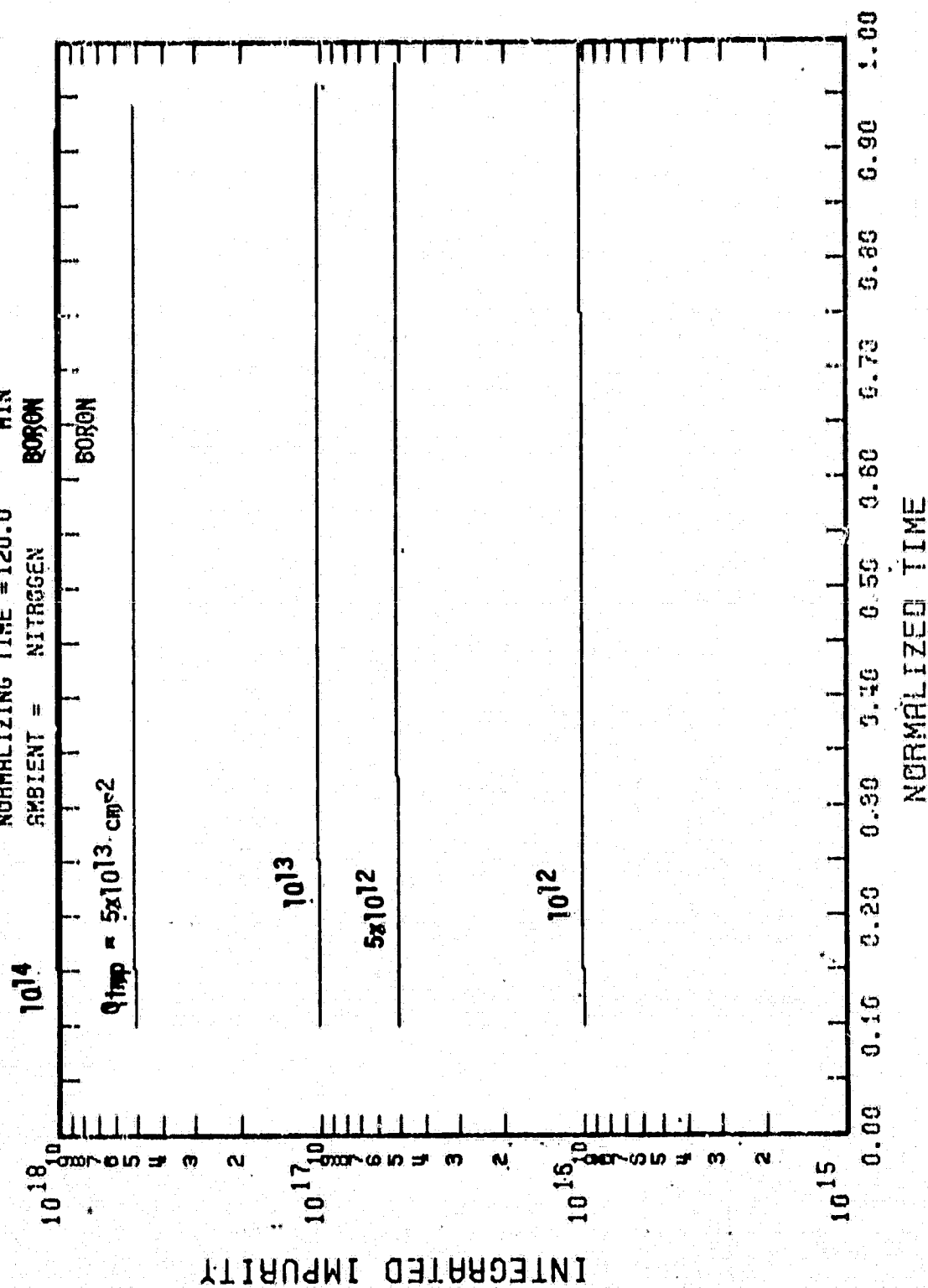


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 NORMALIZING TIME = 120.0 MIN
 AMBIENT = NITROGEN BORON



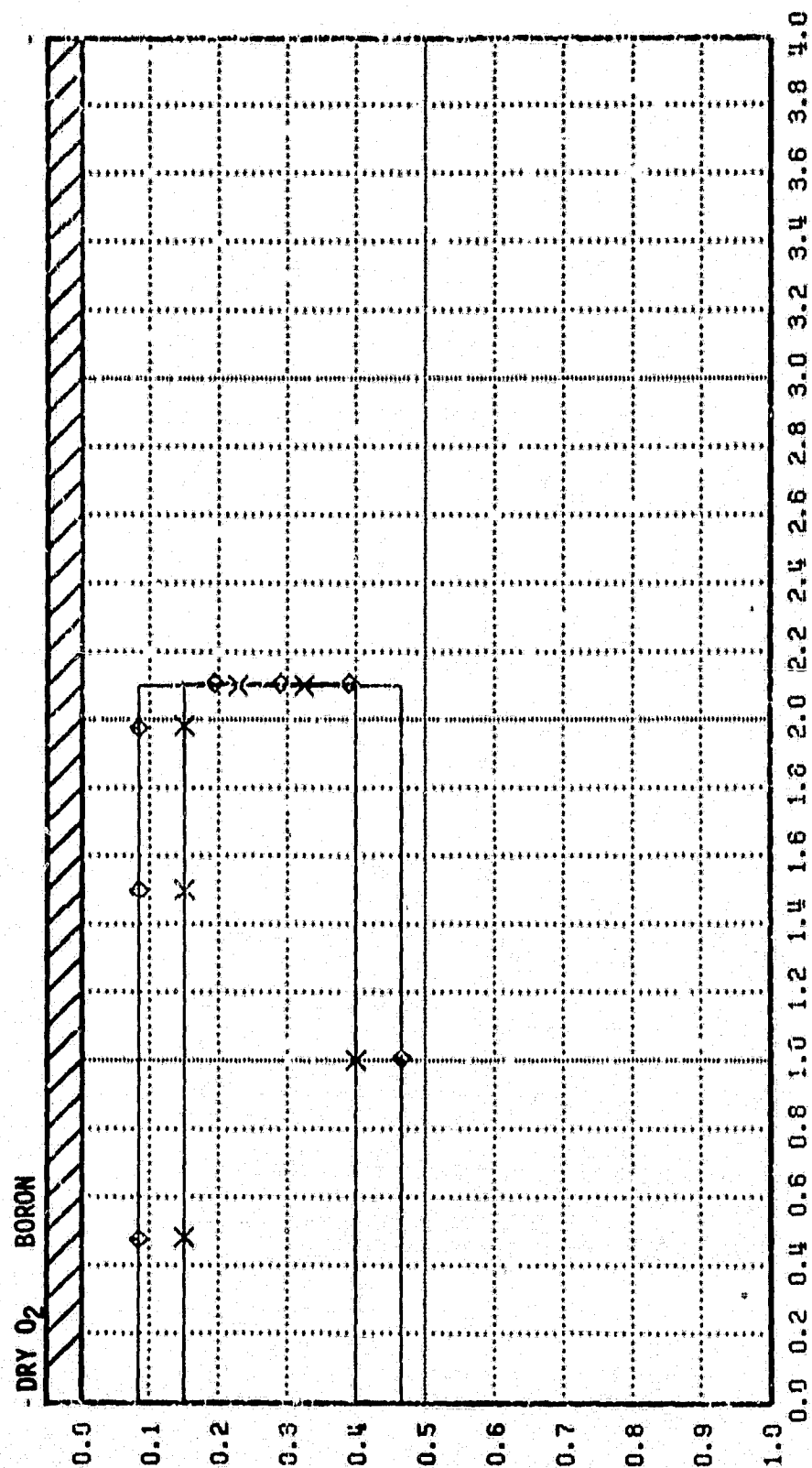


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 NORMALIZING TIME = 120.0 MIN
 AMBIENT = NITROGEN BORON
 BORON

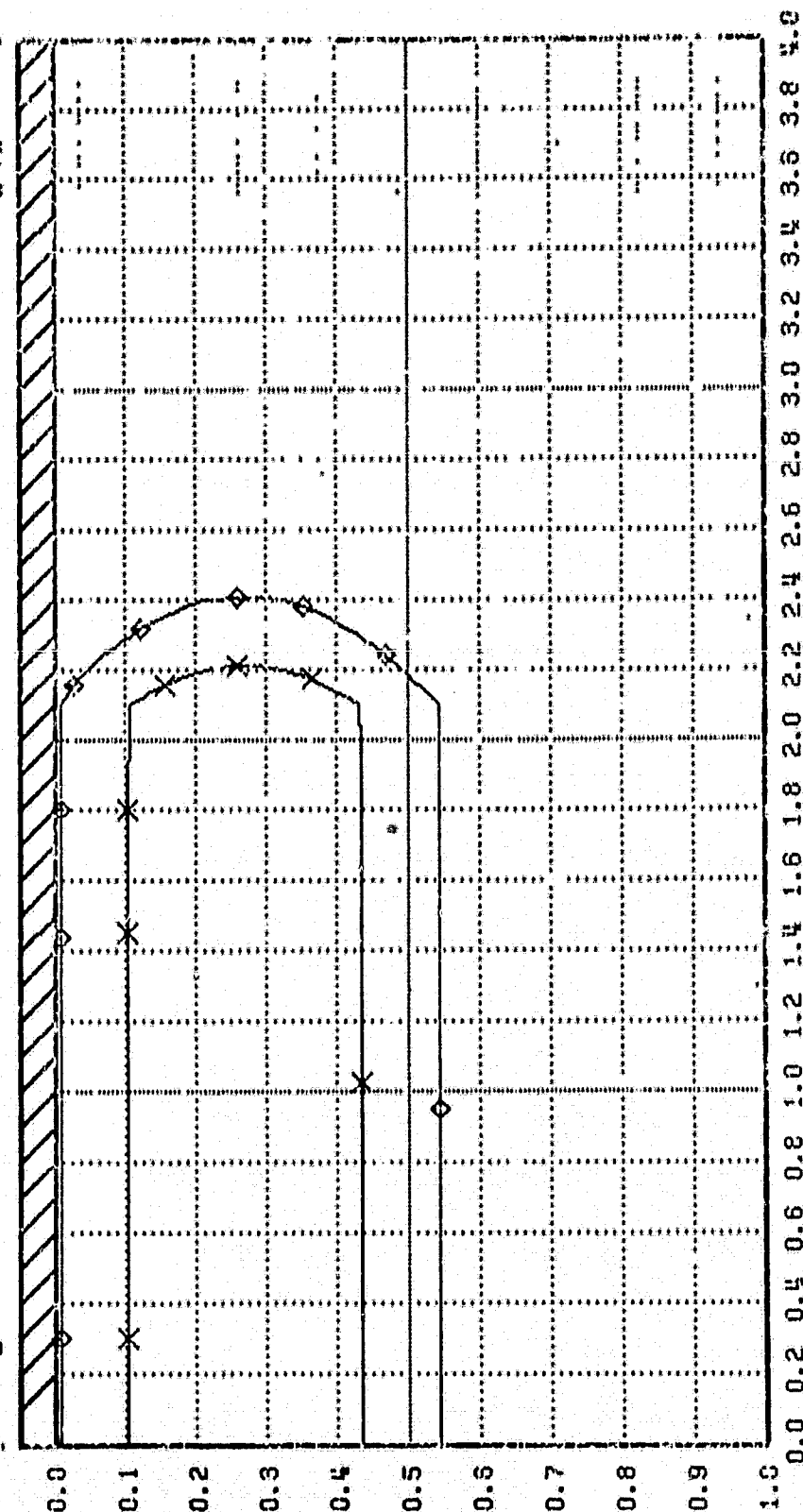


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 TEMPERATURE = 1000.
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 TIME = 0.00

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 □ - 1.0E19
 △ - 1.0E18
 + - 1.0E17
 X - 1.0E16
 ◇ - 1.0E15



λ^2
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 TIME STEP = 1000.
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 DRY O₂ BORON = 1440.00

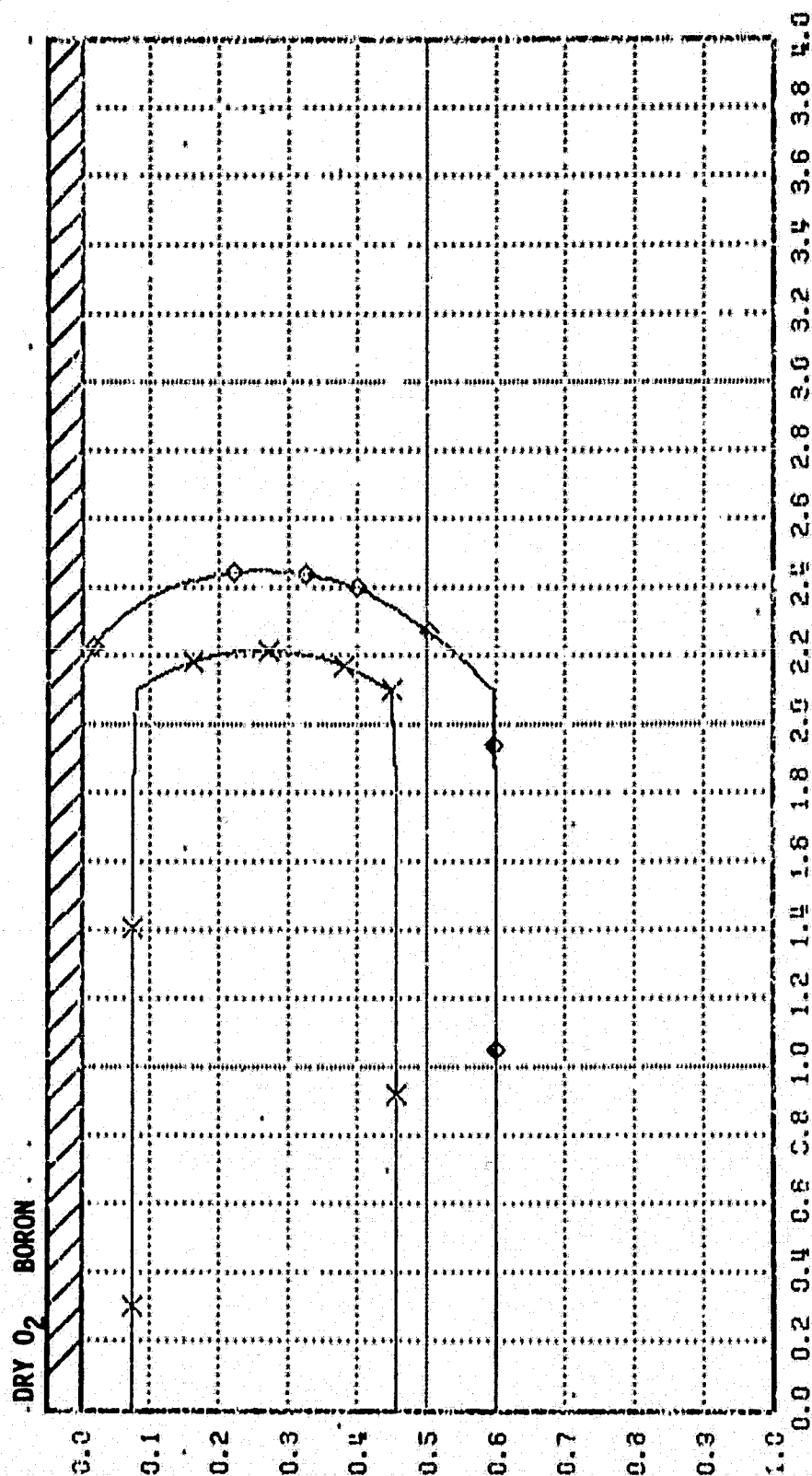


λ^2
 TEMPERATURE
 TIME STEP
 TIME

= 0.0000
 = 1000.
 = 40
 = 2880.00

E
 O
 A
 +
 X
 ◇

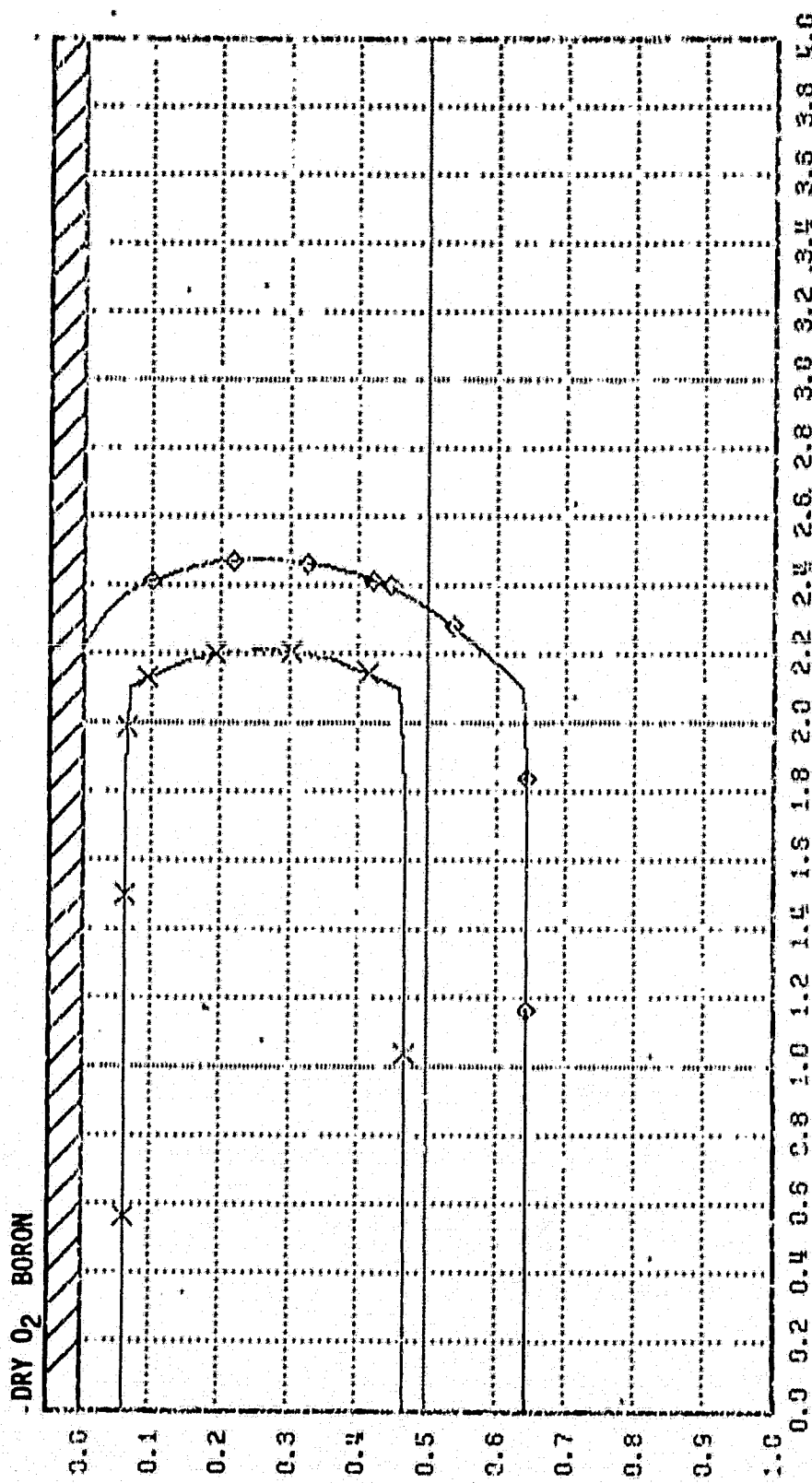
- 1.0E20
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 - 1.0E16
 - 1.0E15



χ^2
 TEMPERATURE
 TIME STEP
 TIME

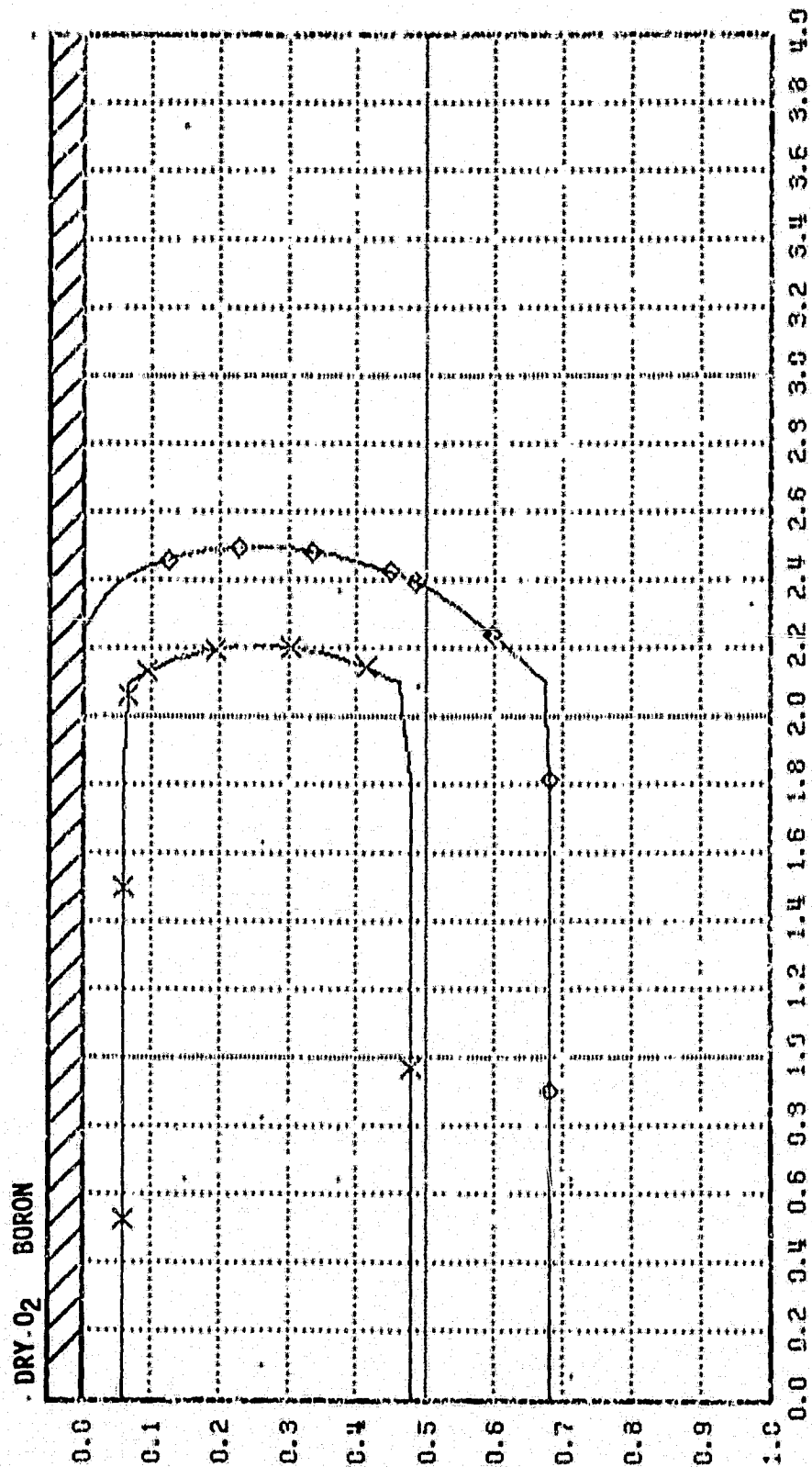
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 = 1000.
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 = 4320.00

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 + - 1.0517
 X - 1.0519
 ◇ - 1.0515



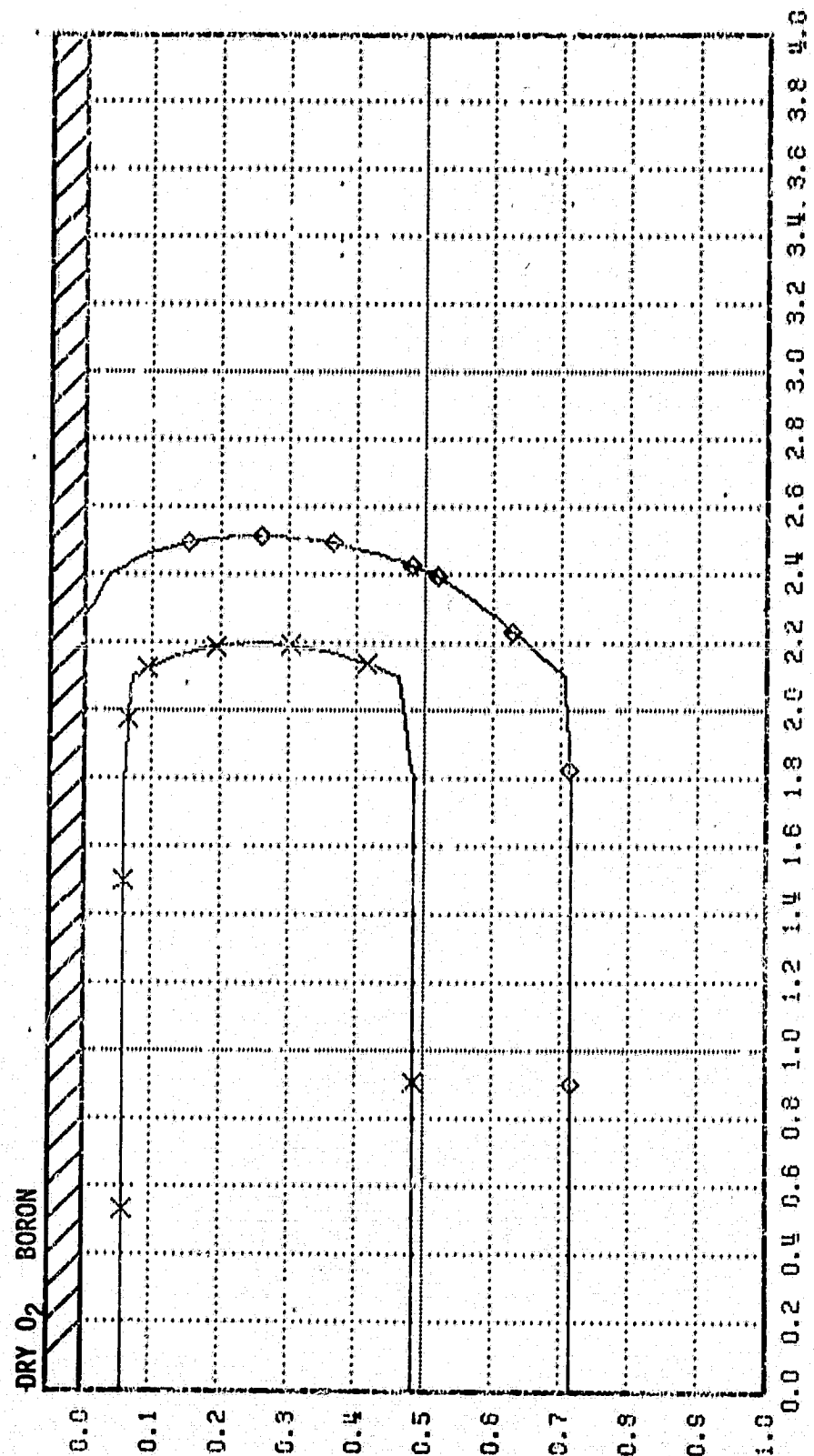
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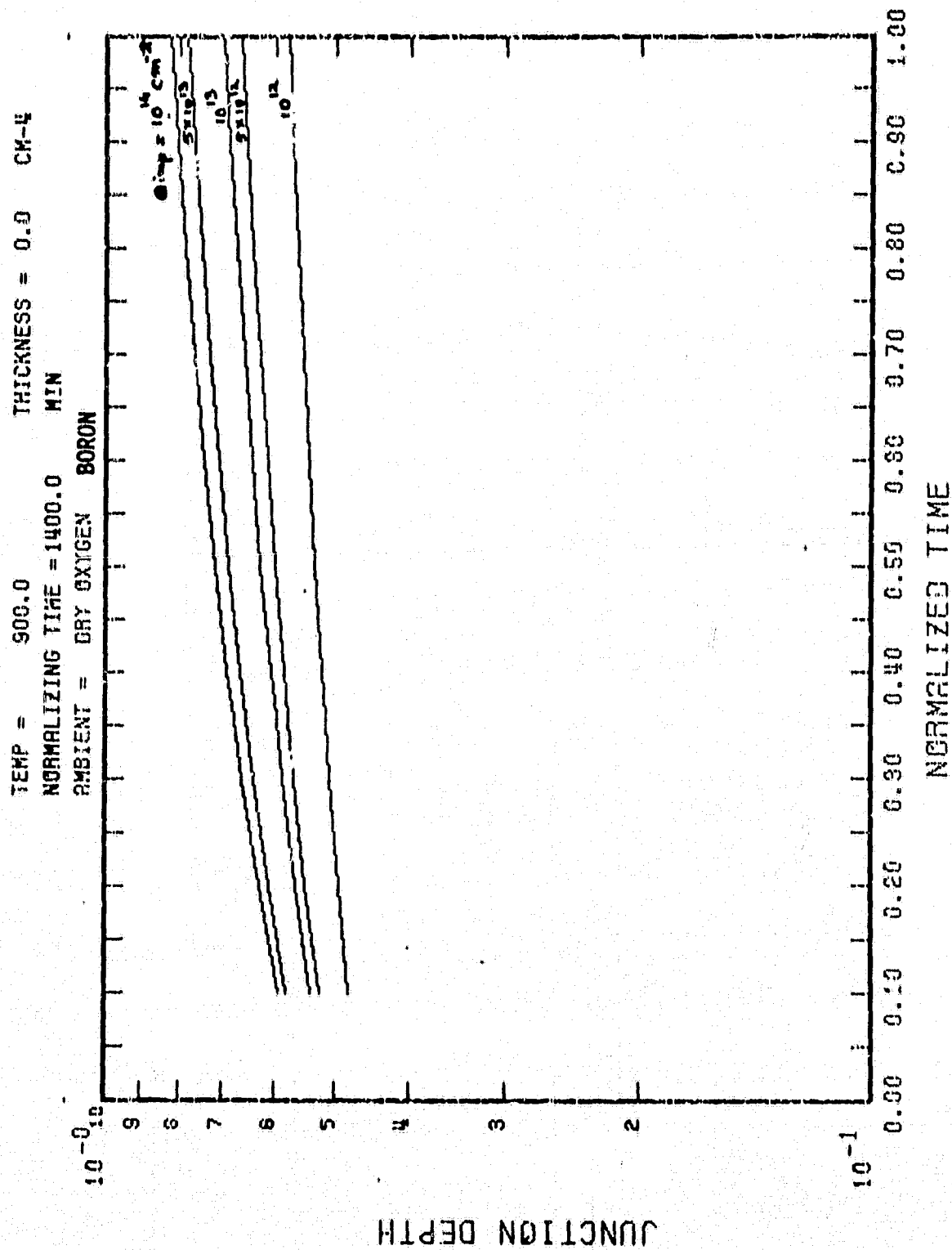
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 - 1.0E17
 - 1.0E16
 - 1.0E15



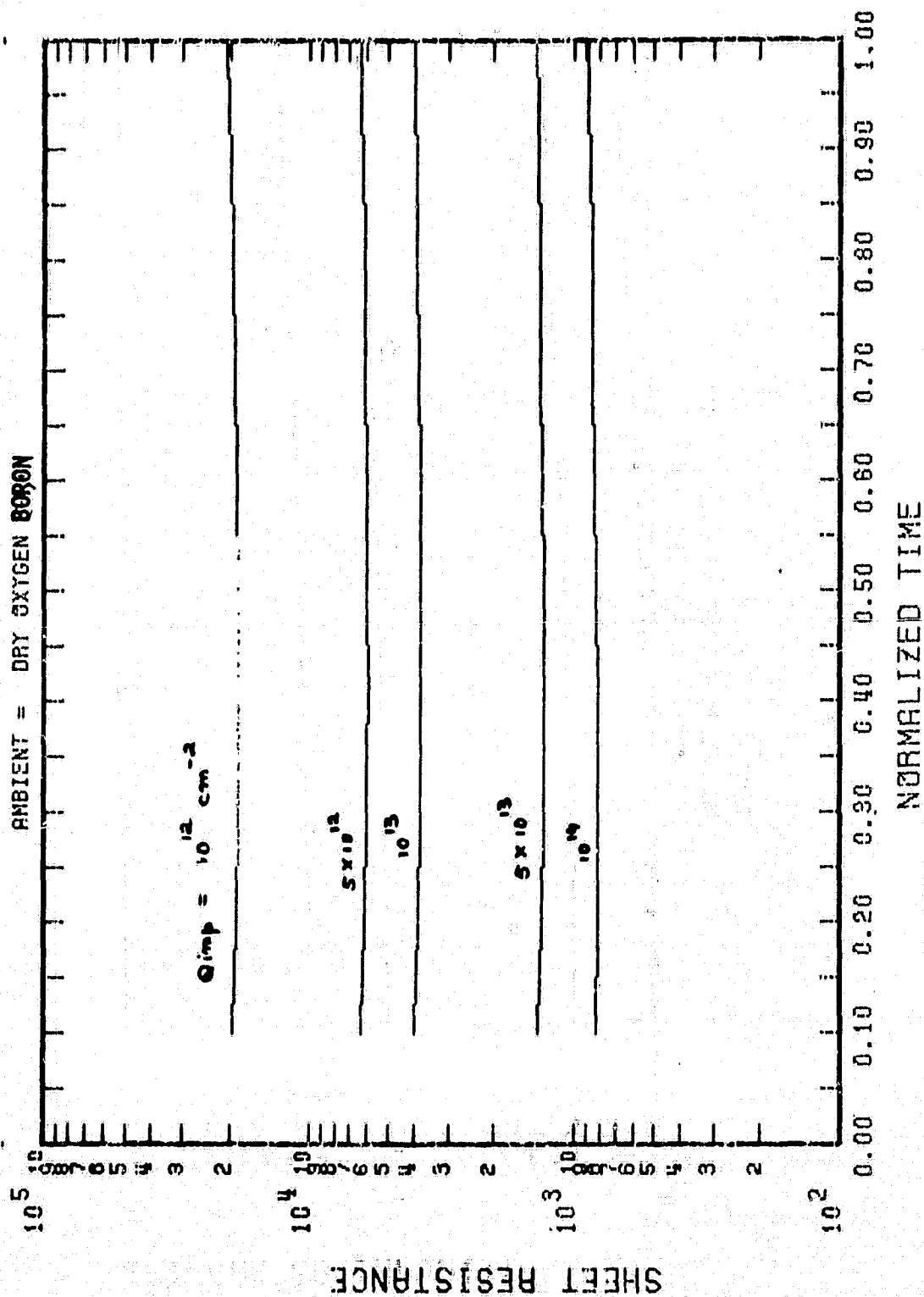
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 A - 1.0E18
 + - 1.0E17
 X - 1.0E16
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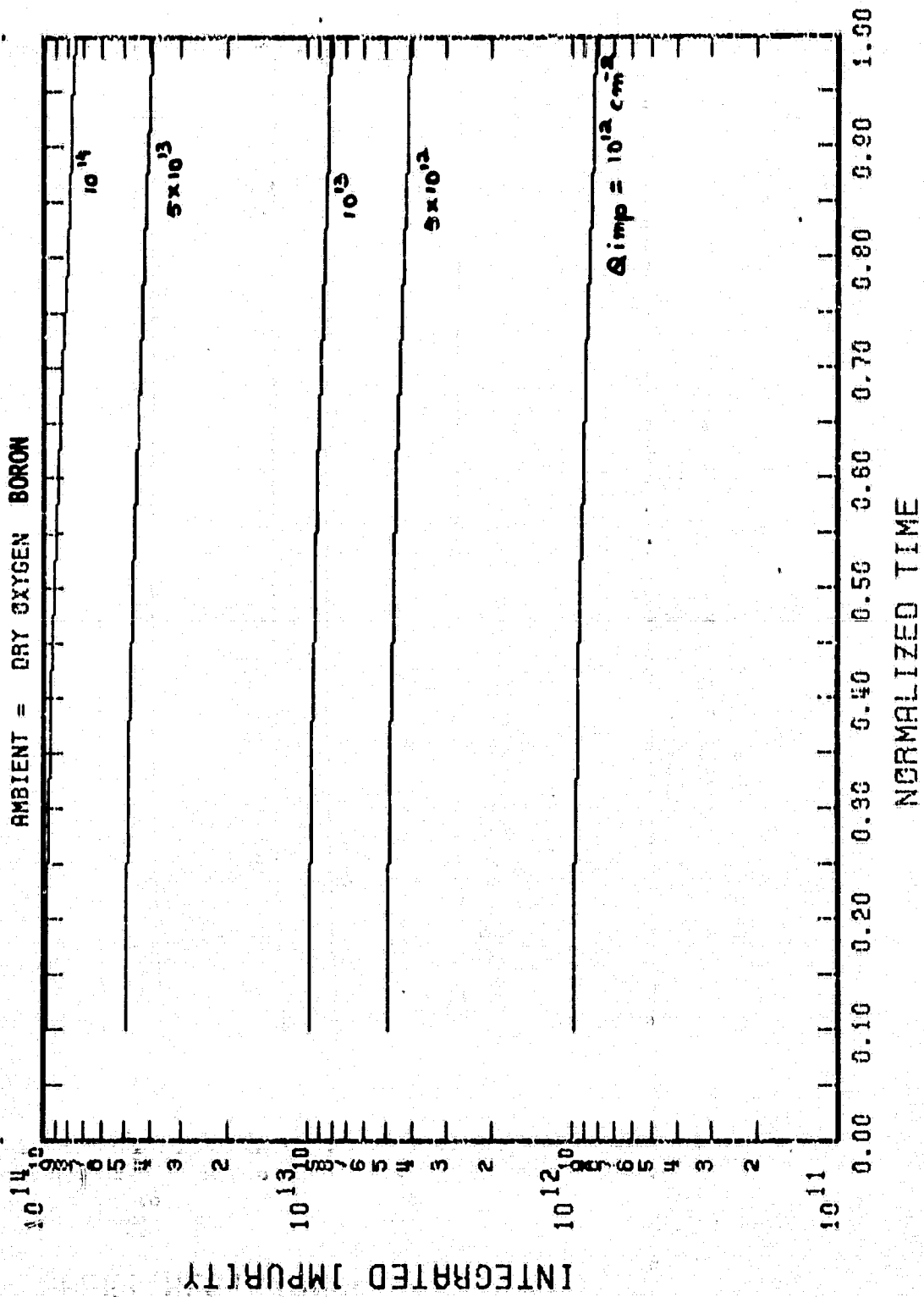




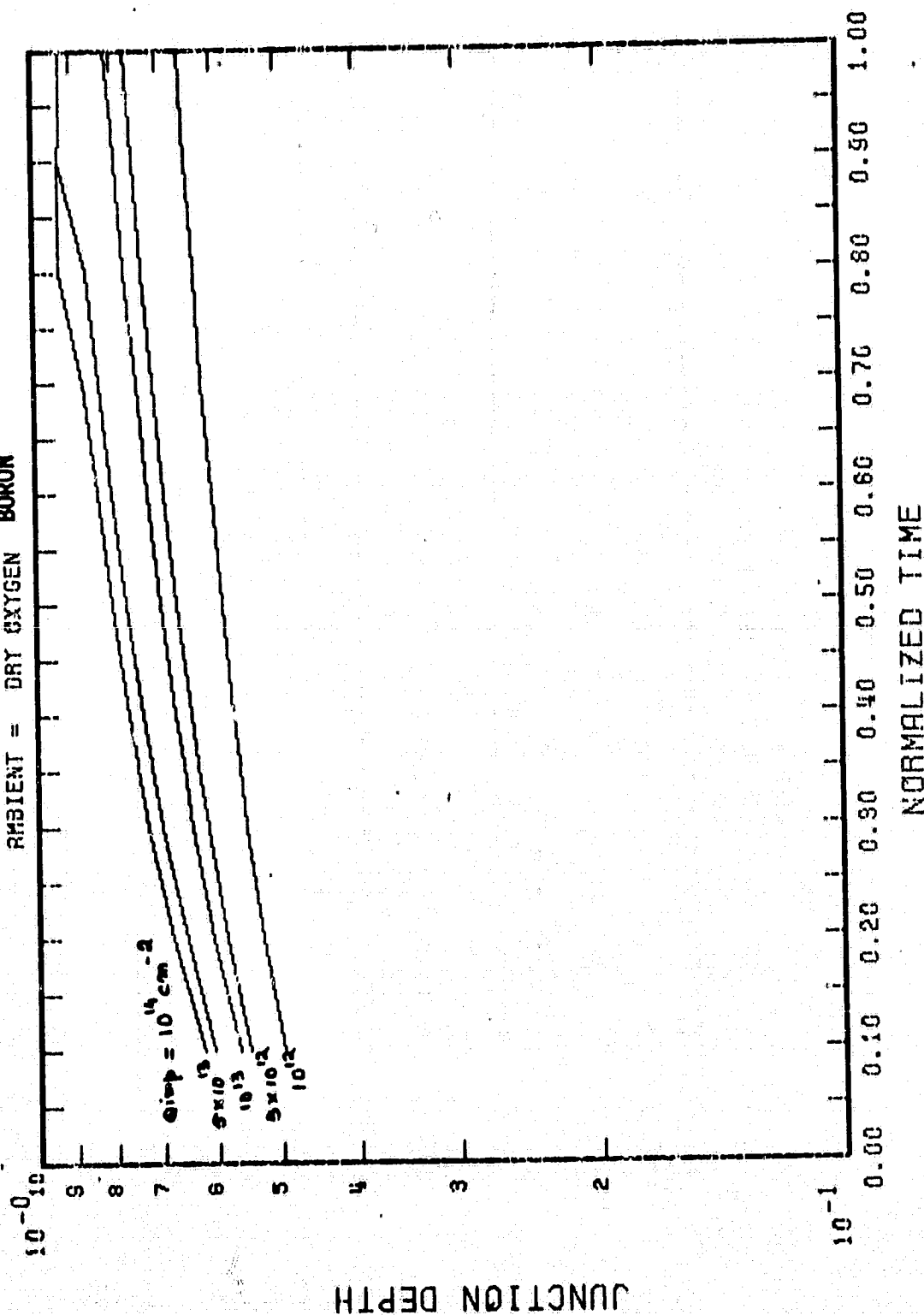
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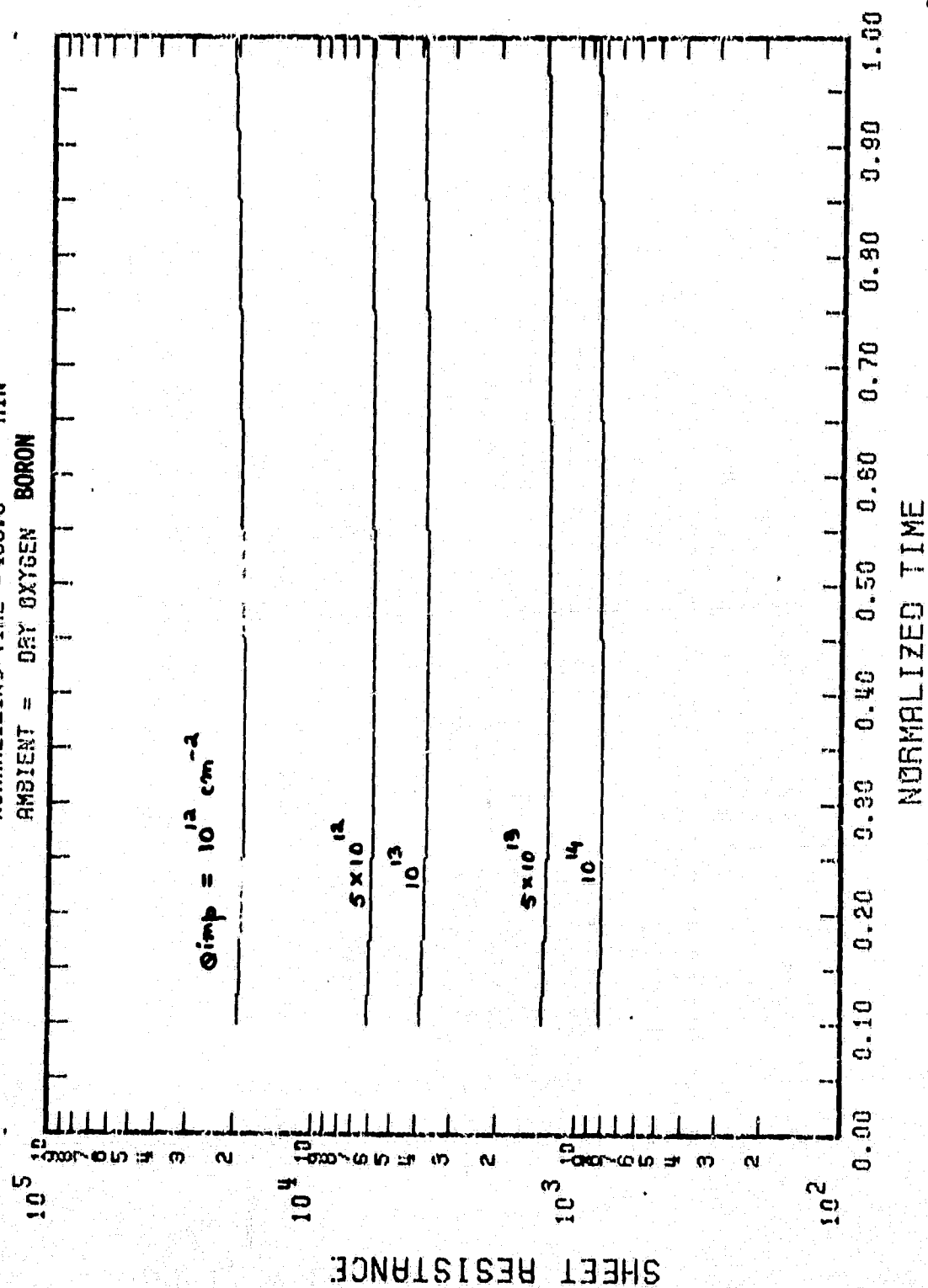
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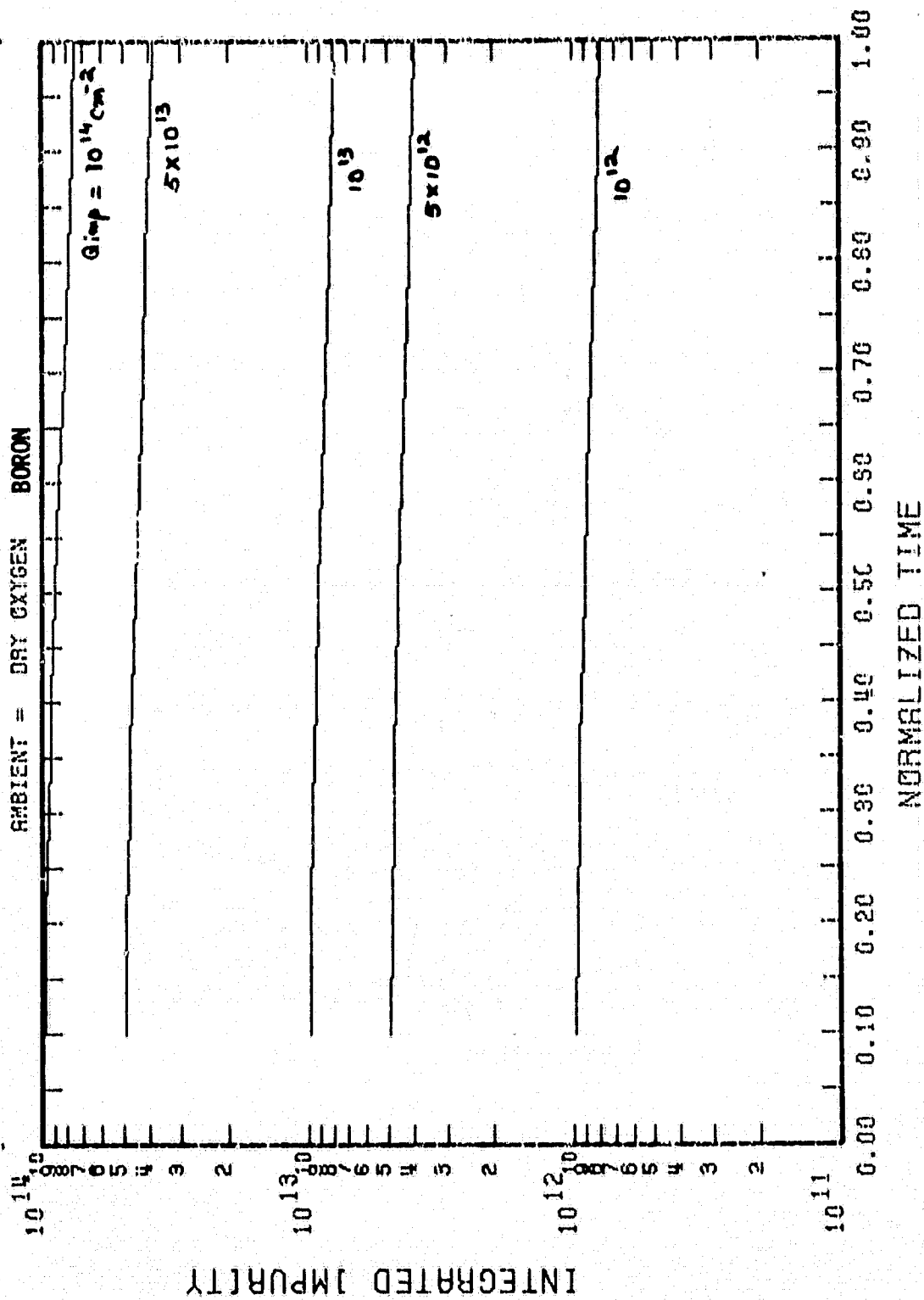
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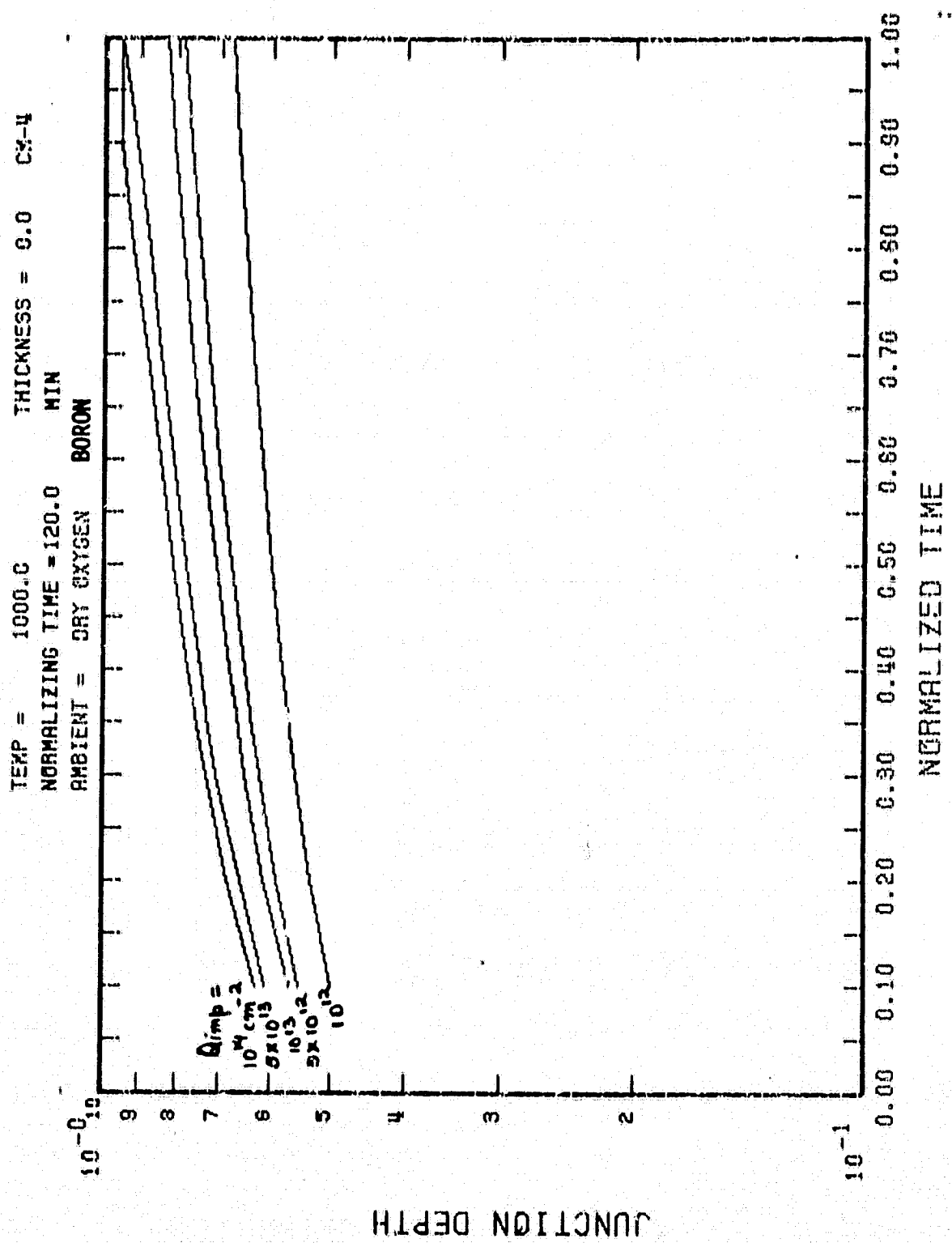


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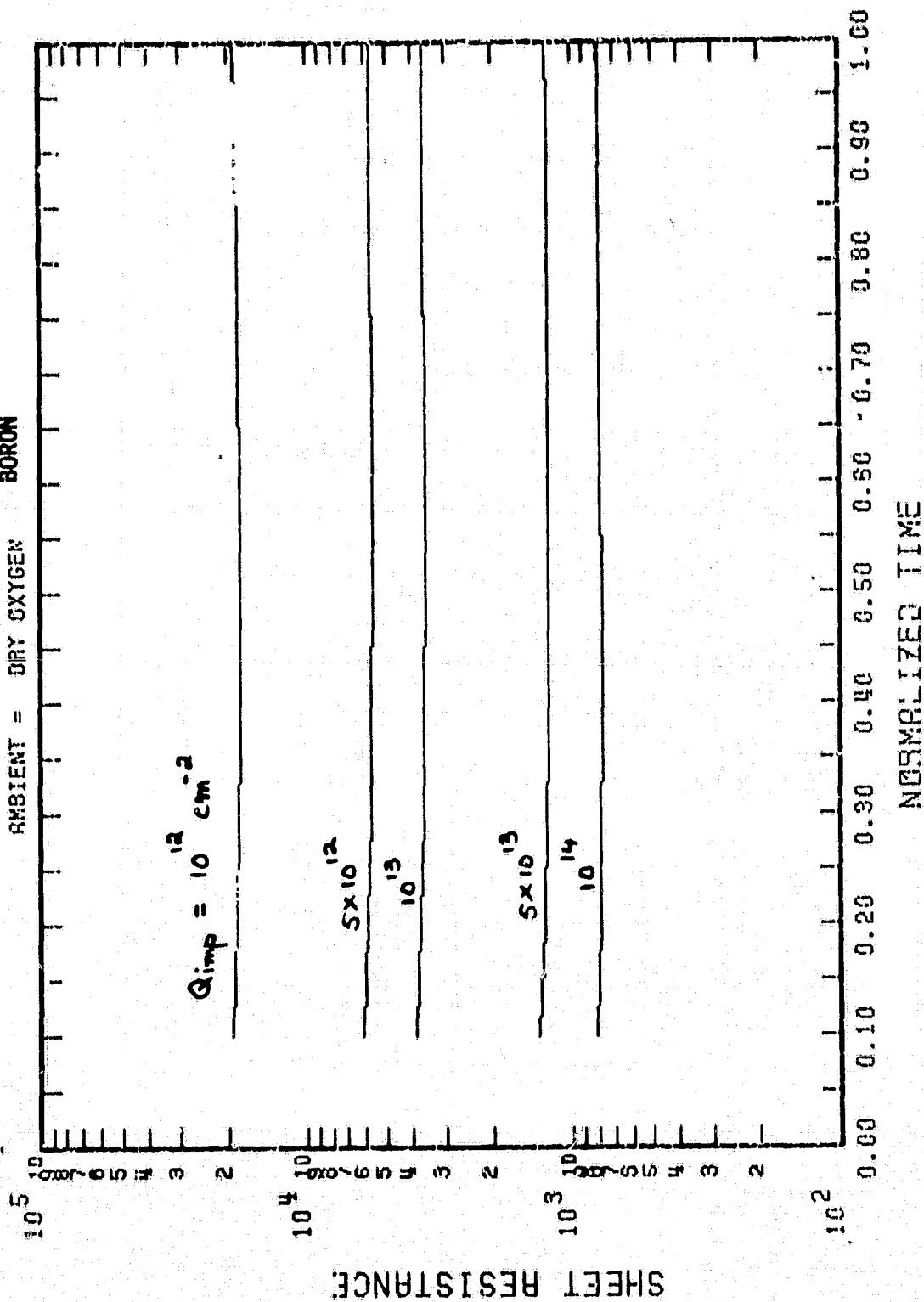


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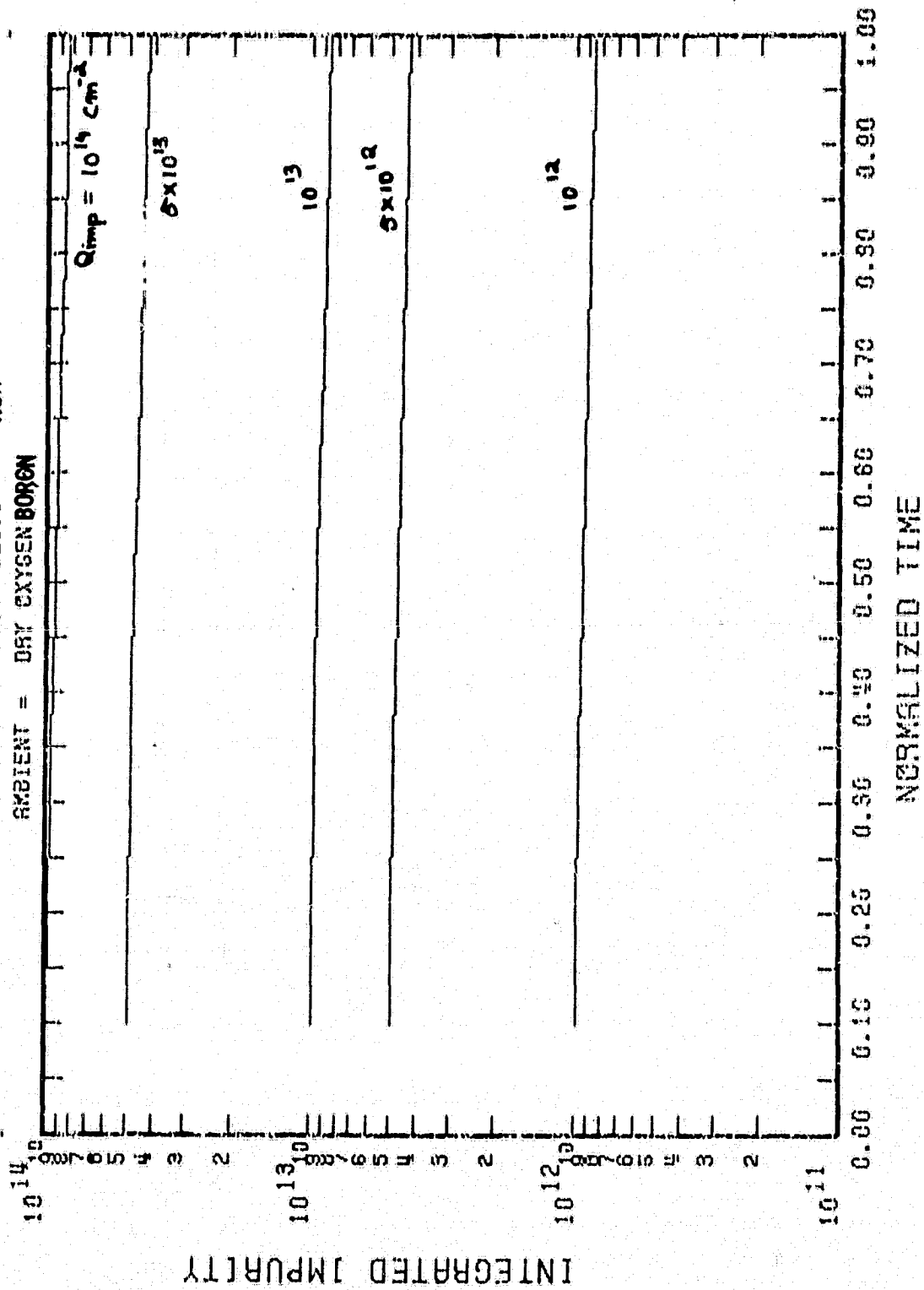


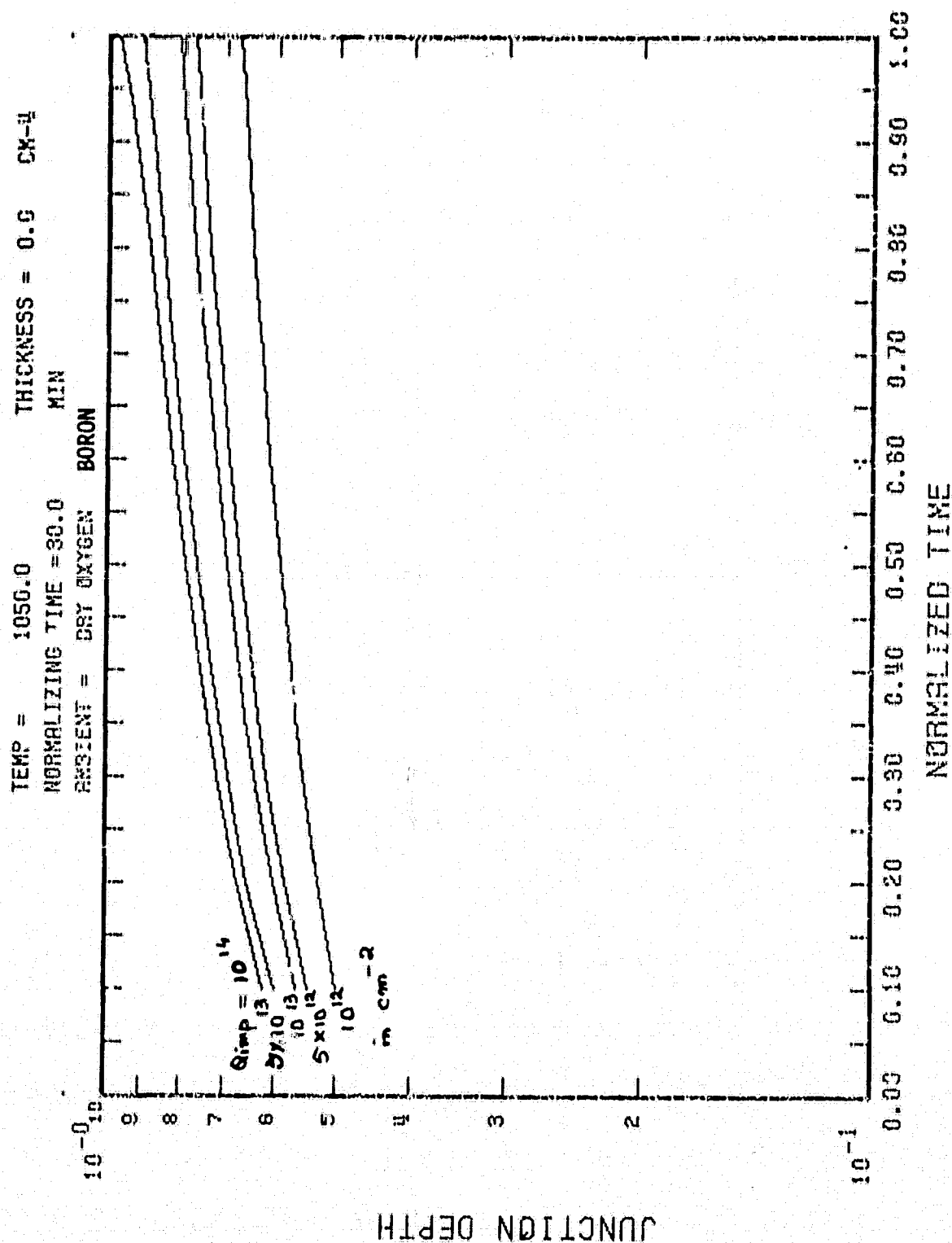


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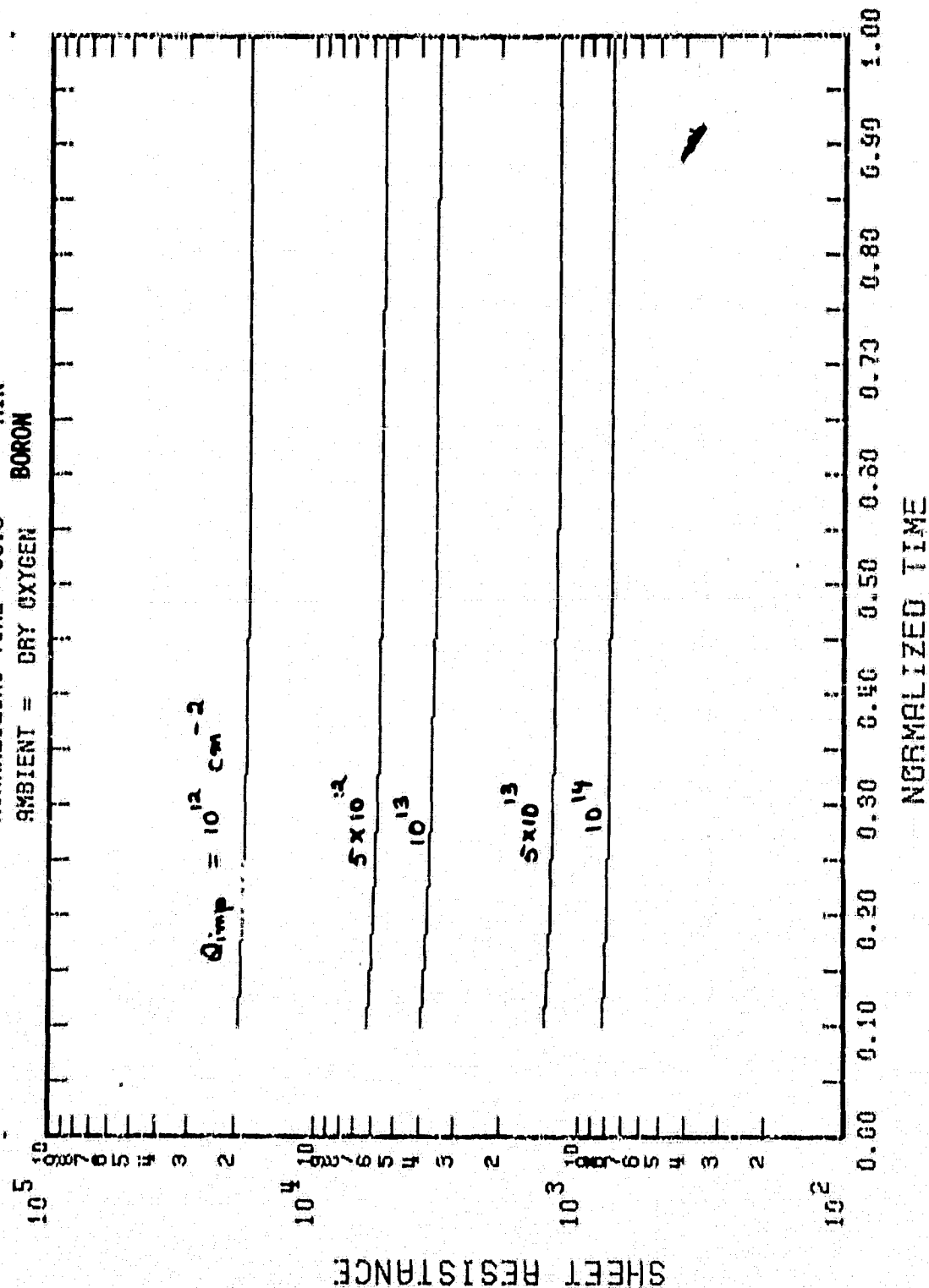


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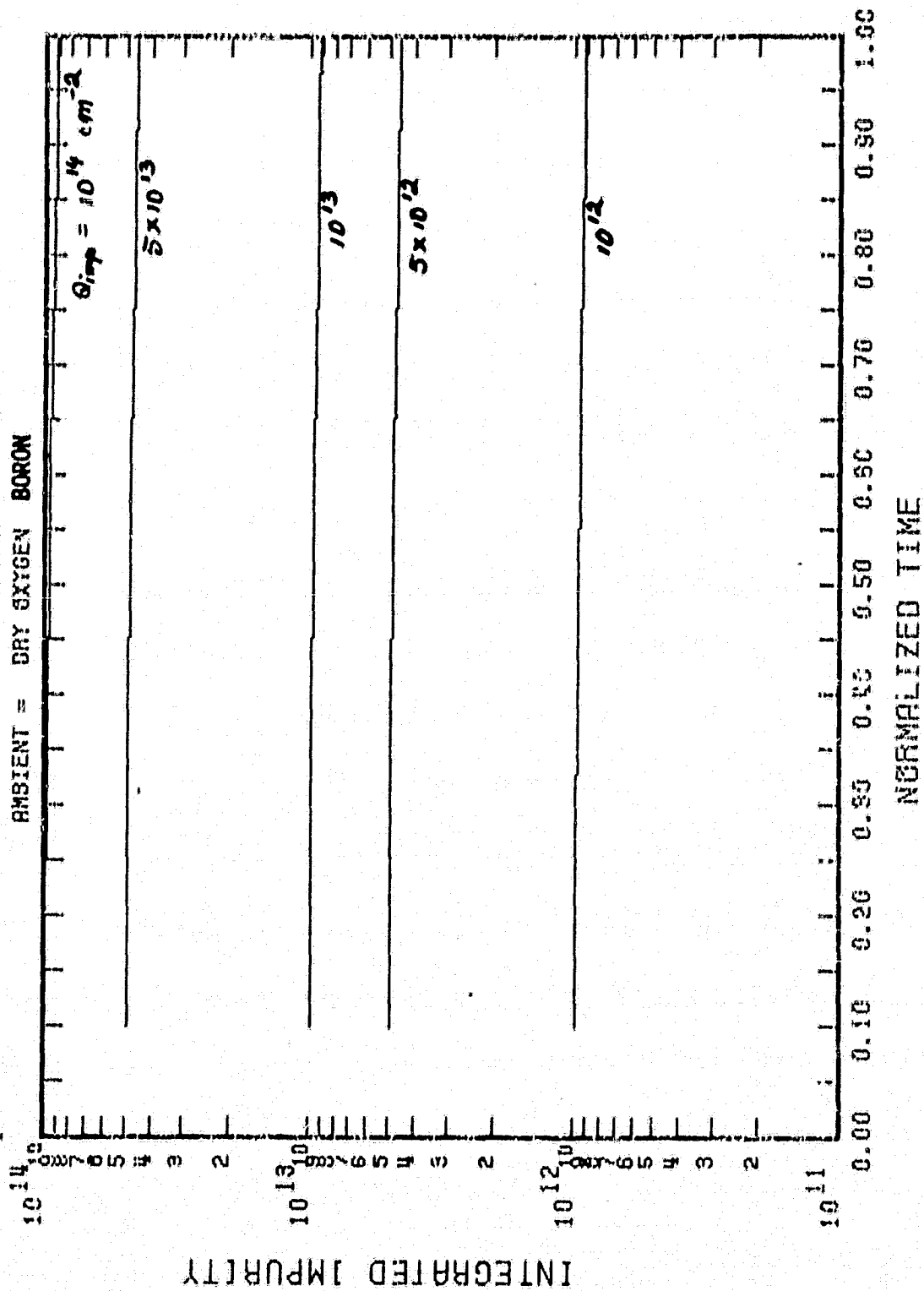




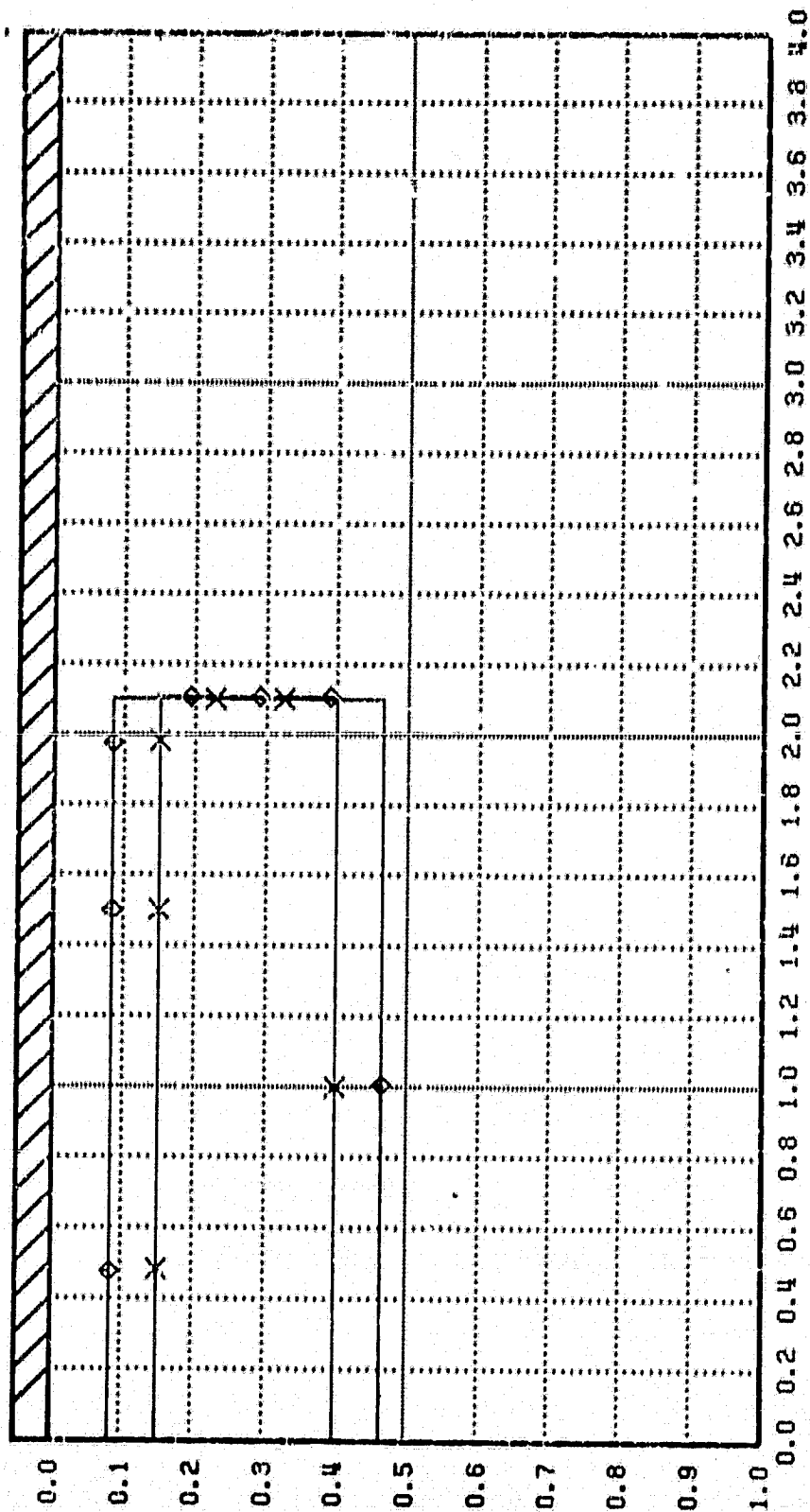
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TEMP = 1050.0
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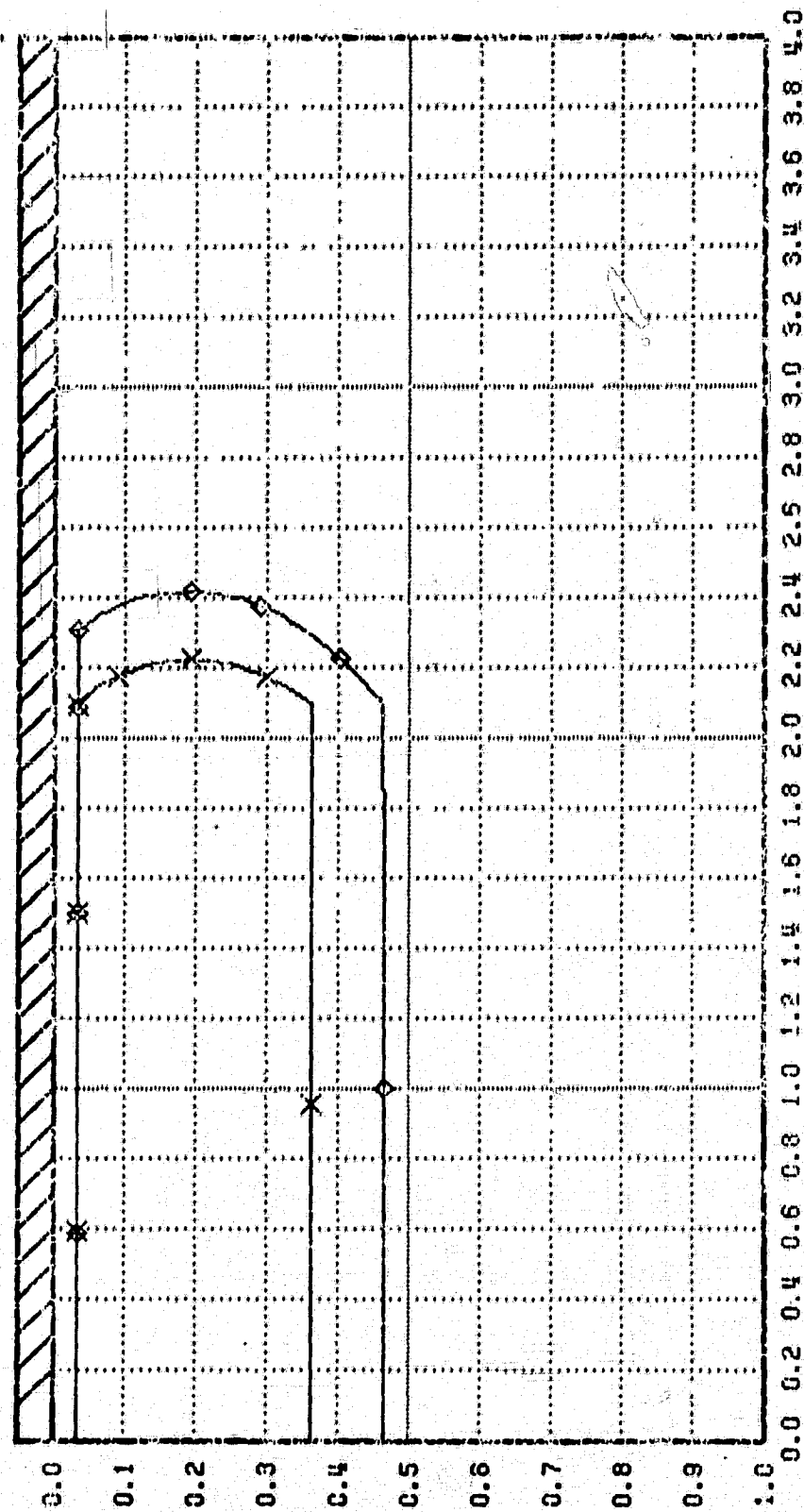


λ^2
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 TIME = 0
 TIME = 0.00
 BORON STEAM
 - 1.0E20
 - 1.0E19
 - 1.0E18
 + 1.0E17
 x 1.0E16
 - 1.0E15



λ^2
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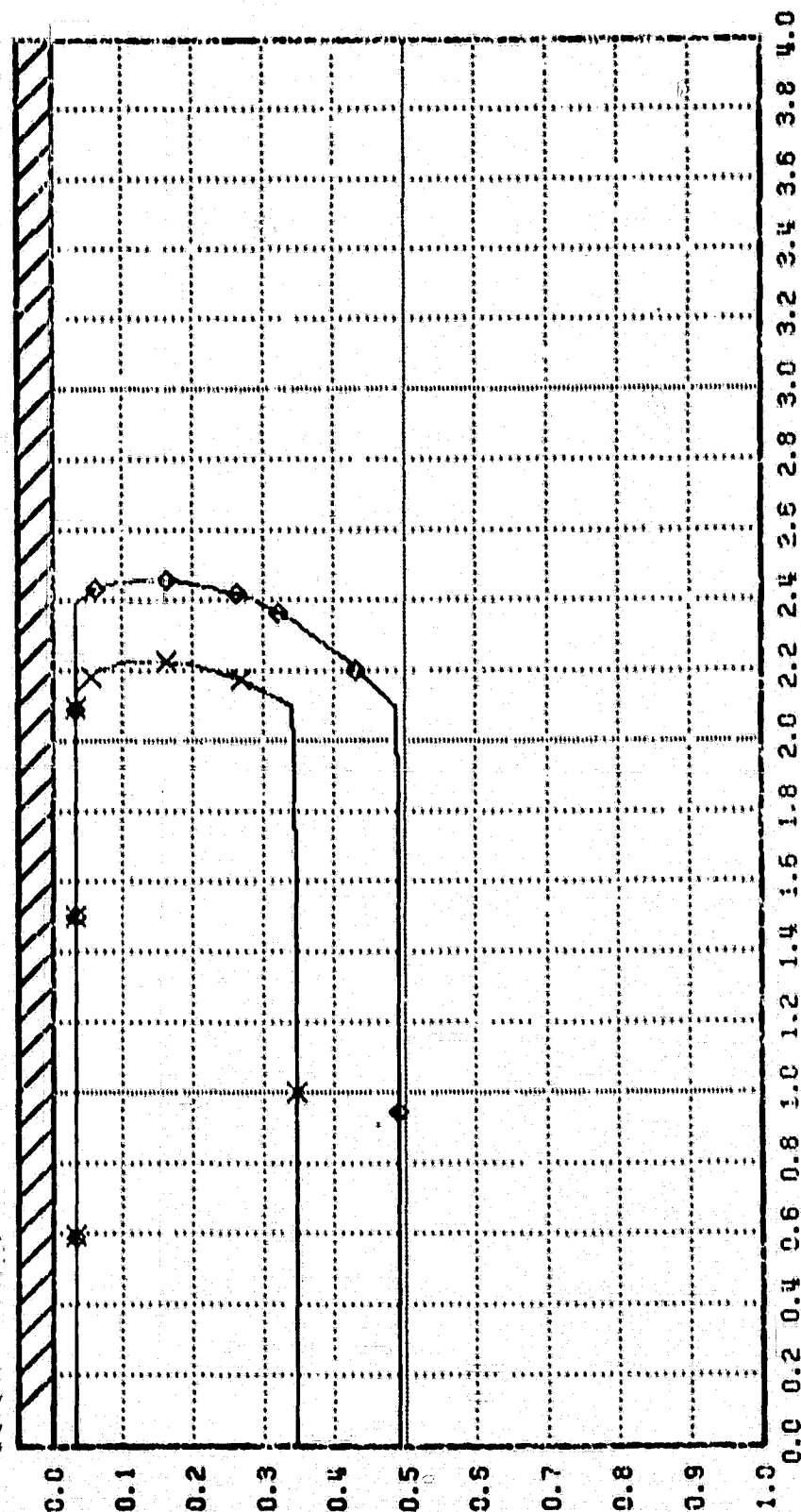
BORON STEAM

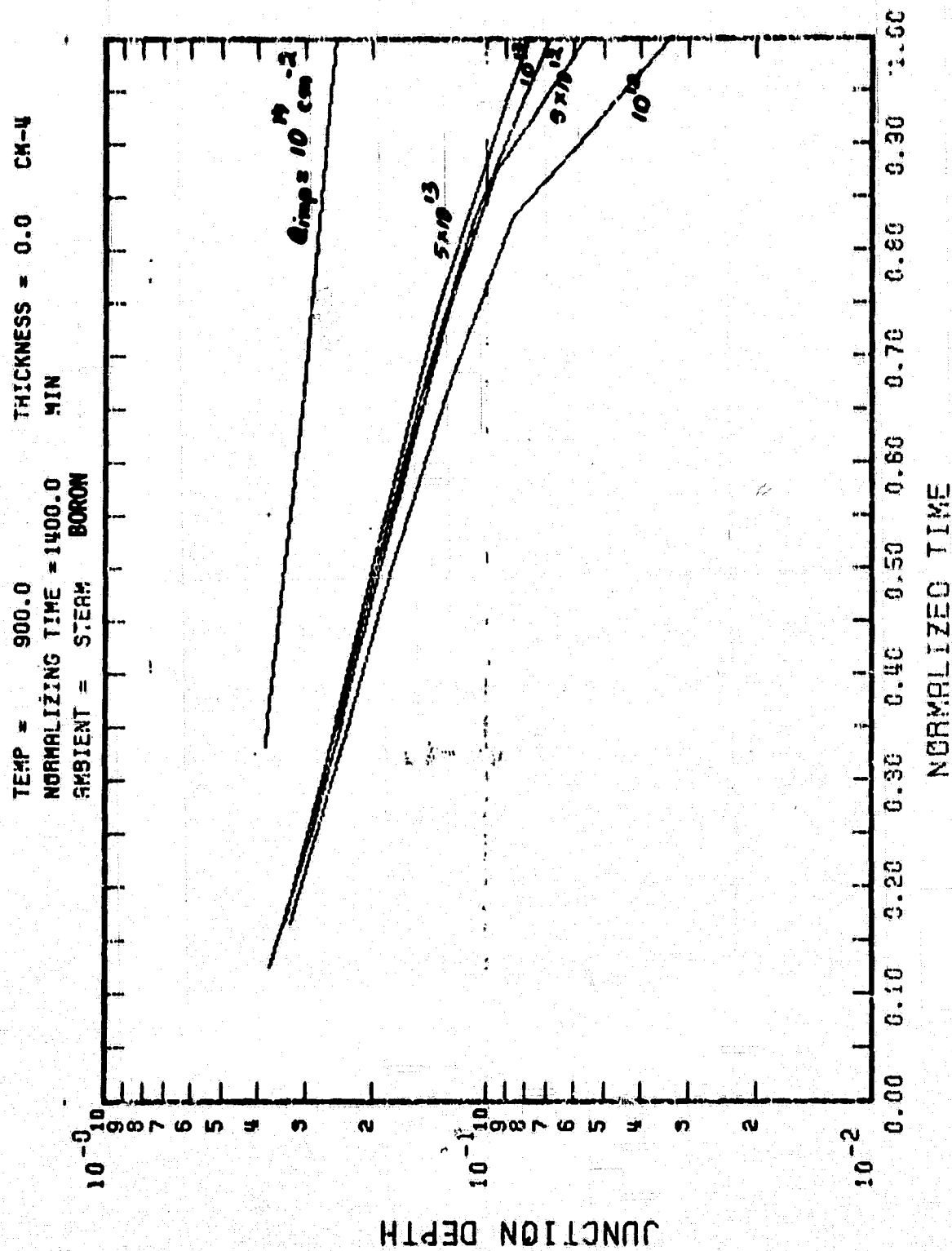


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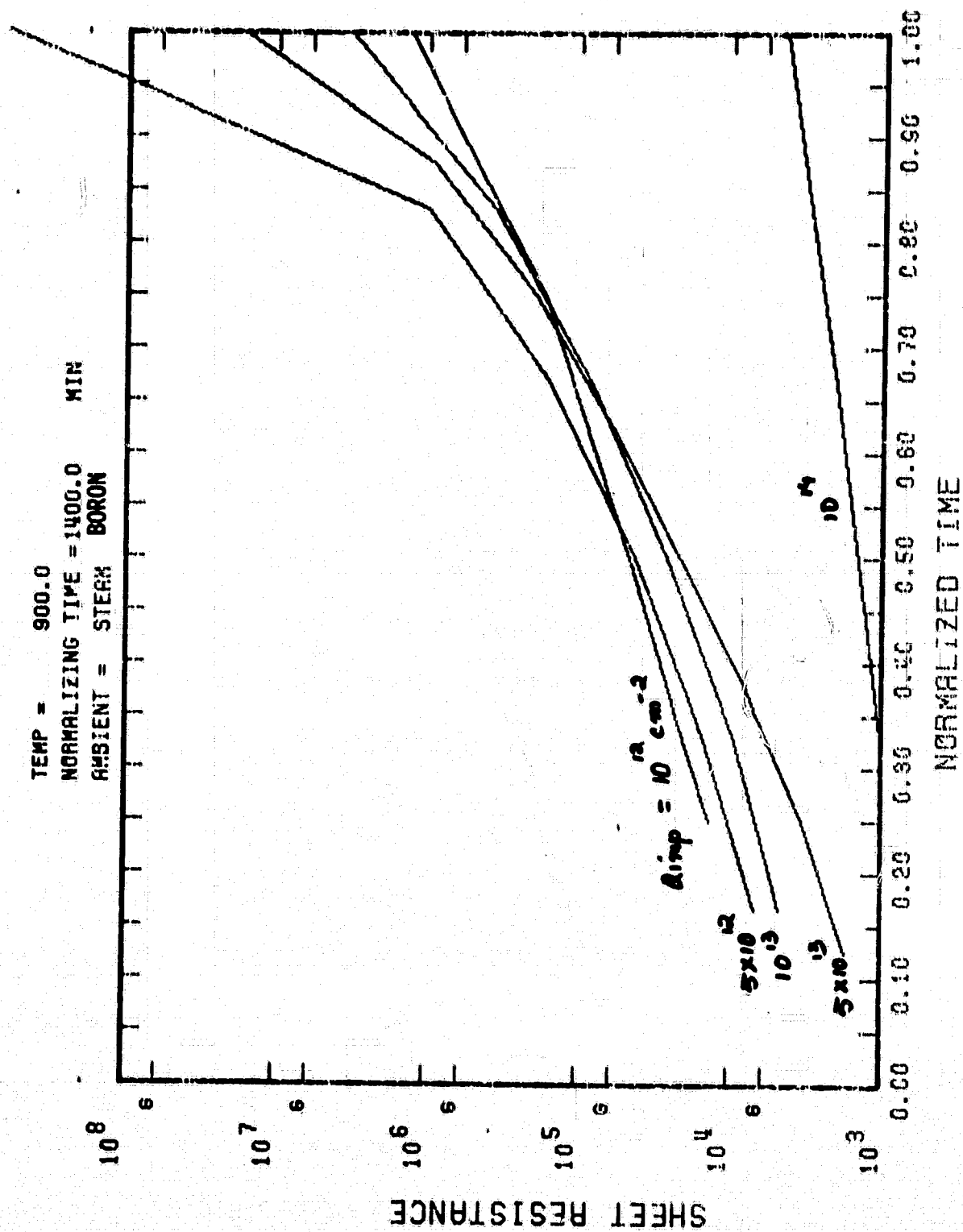
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BORON STEAM

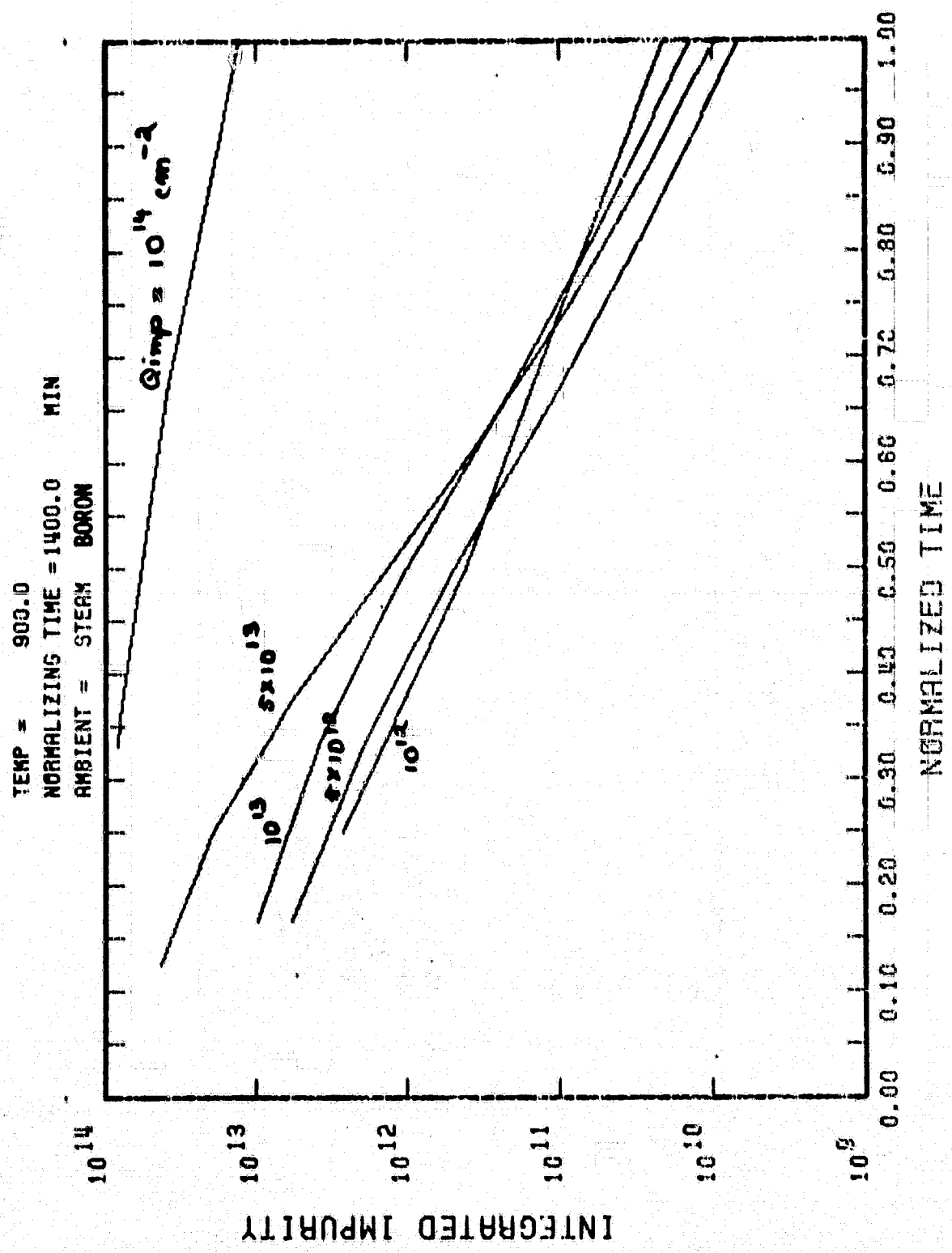




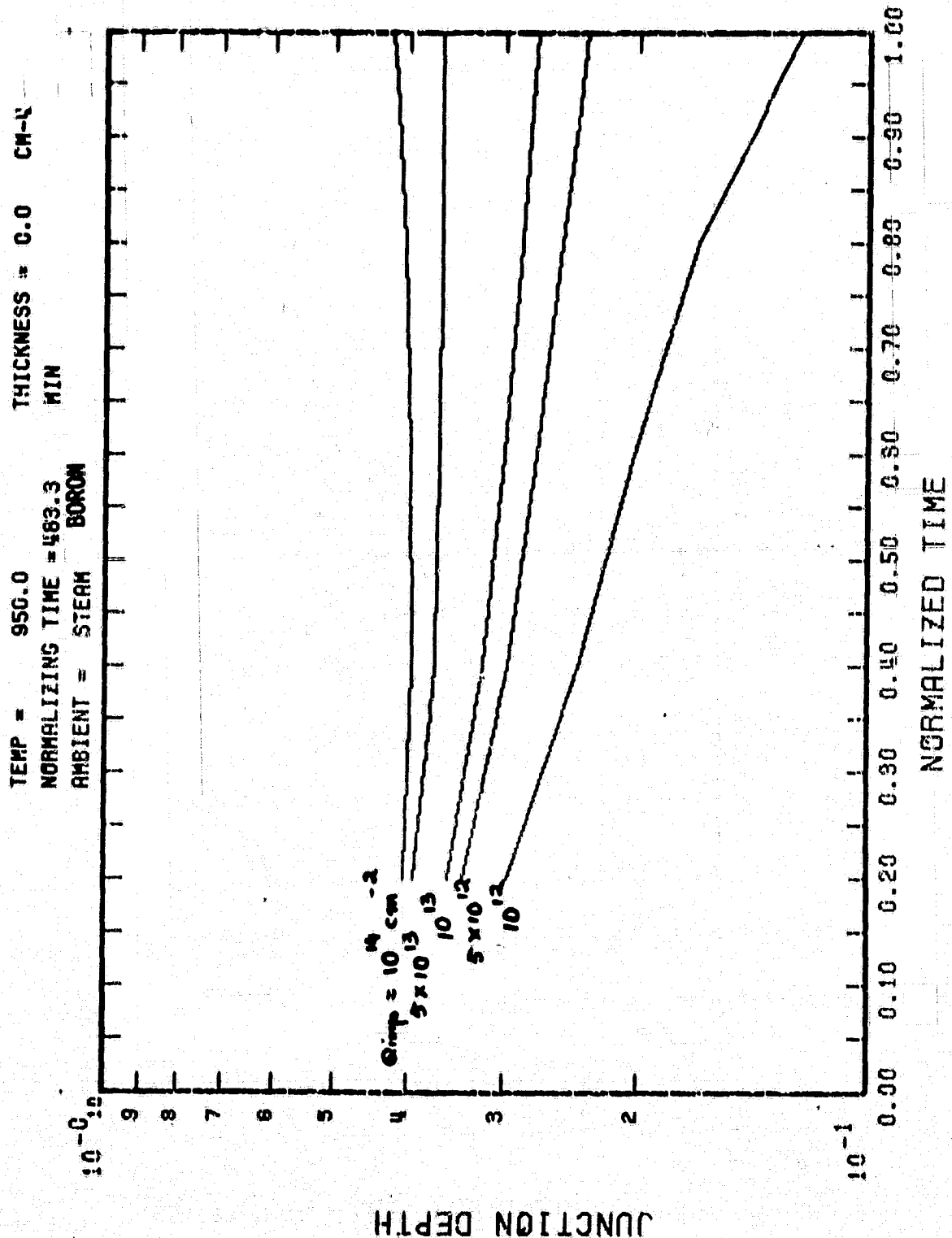
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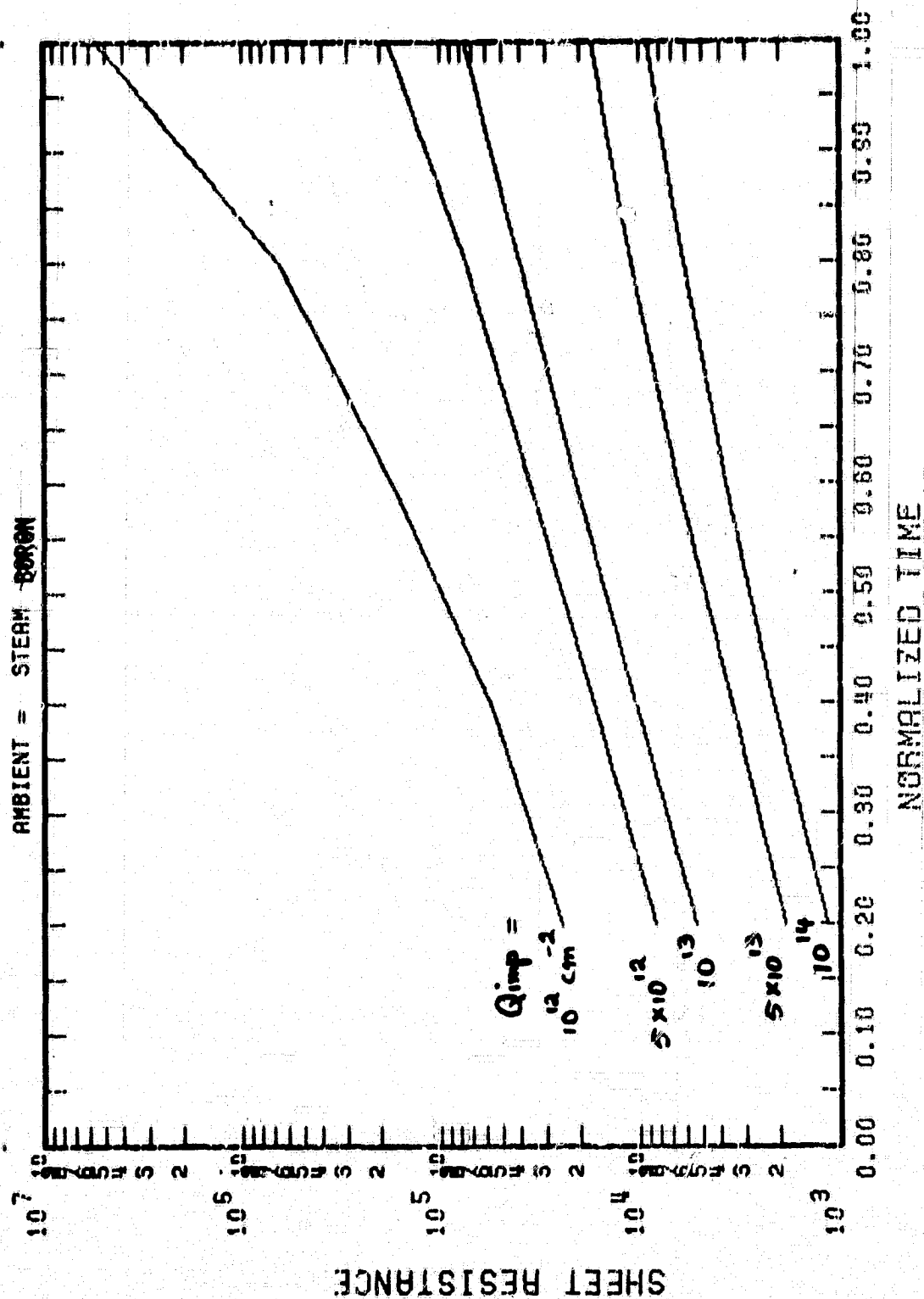
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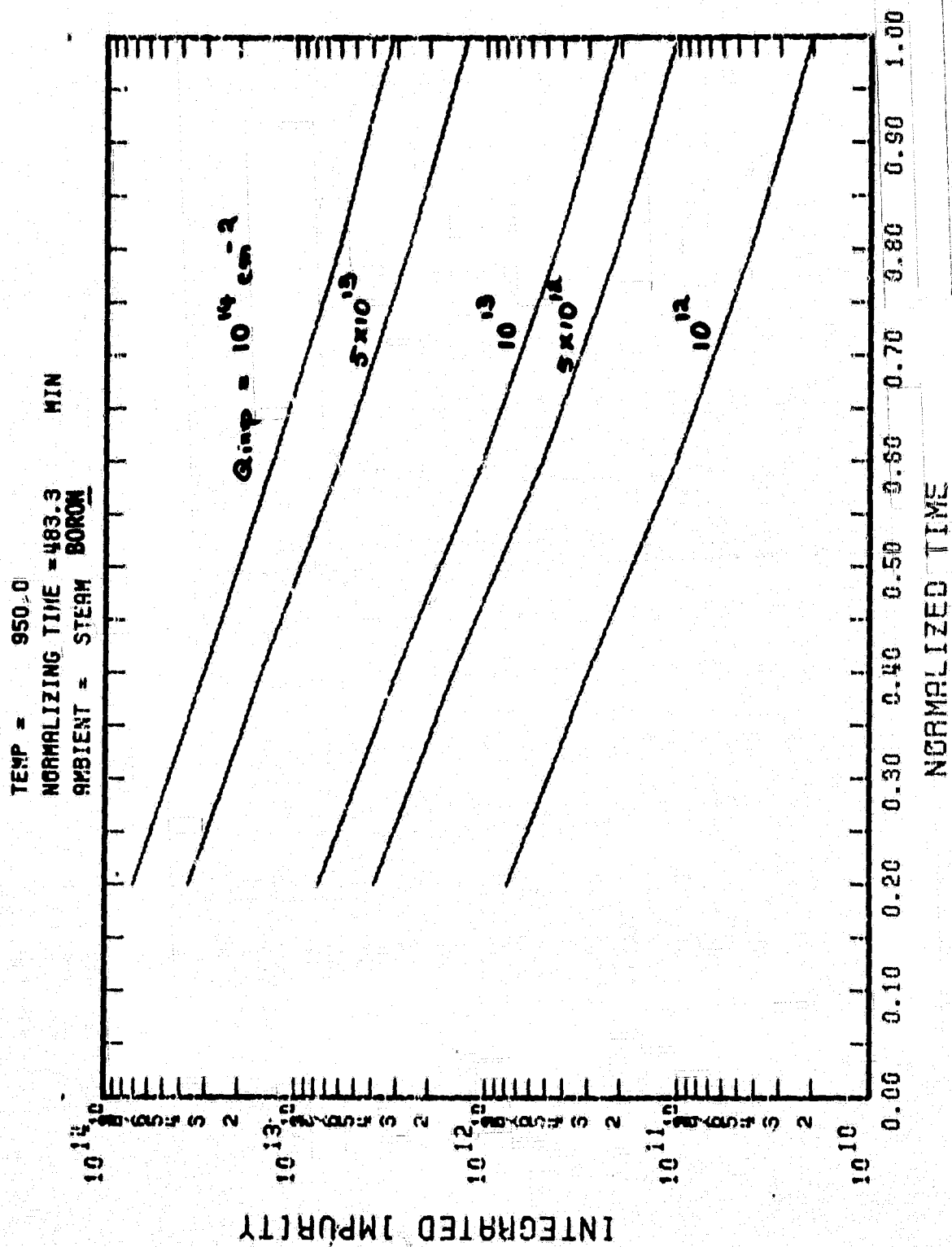
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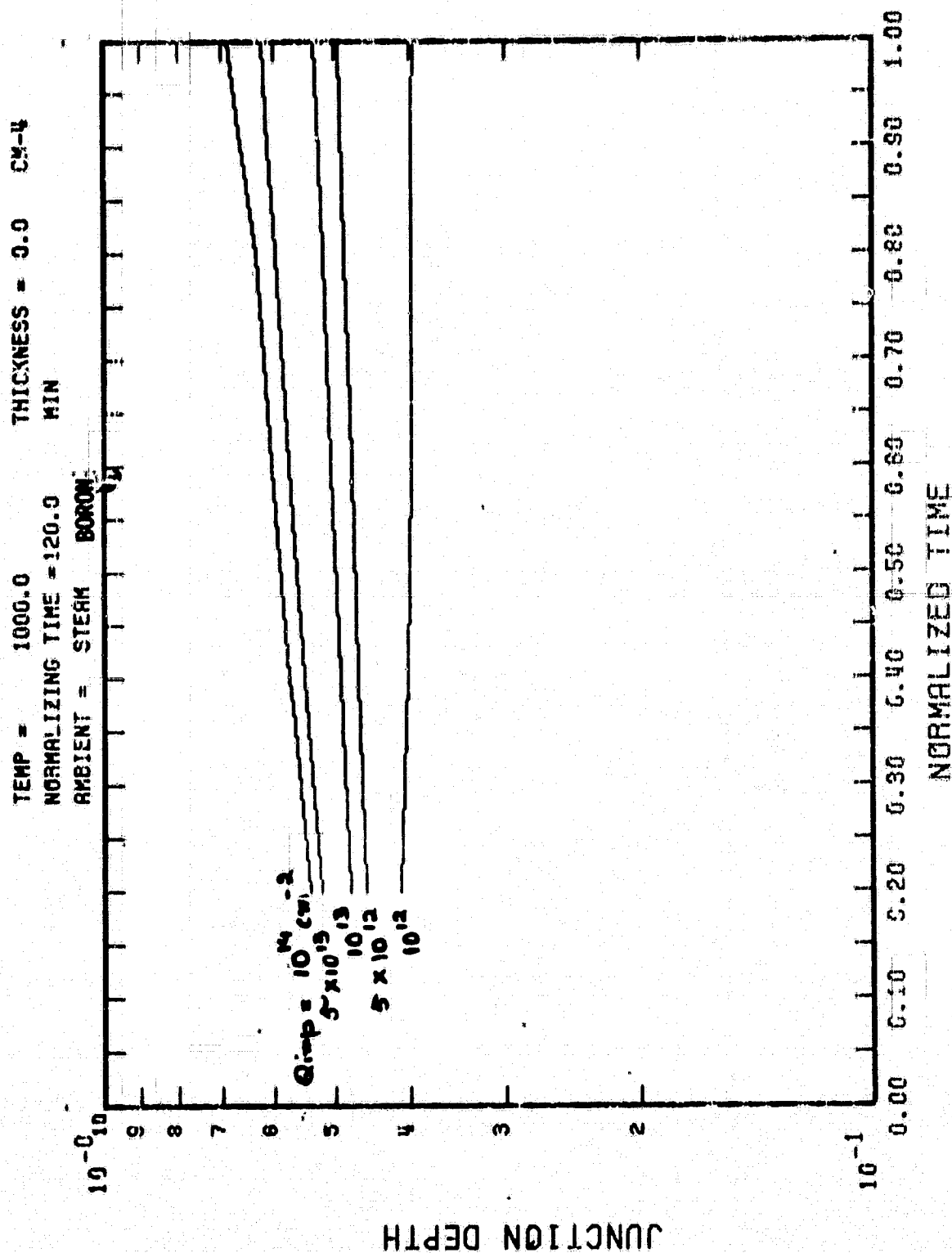


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 NORMALIZING TIME = 483.3 MIN
 AMBIENT = STEAM BORON

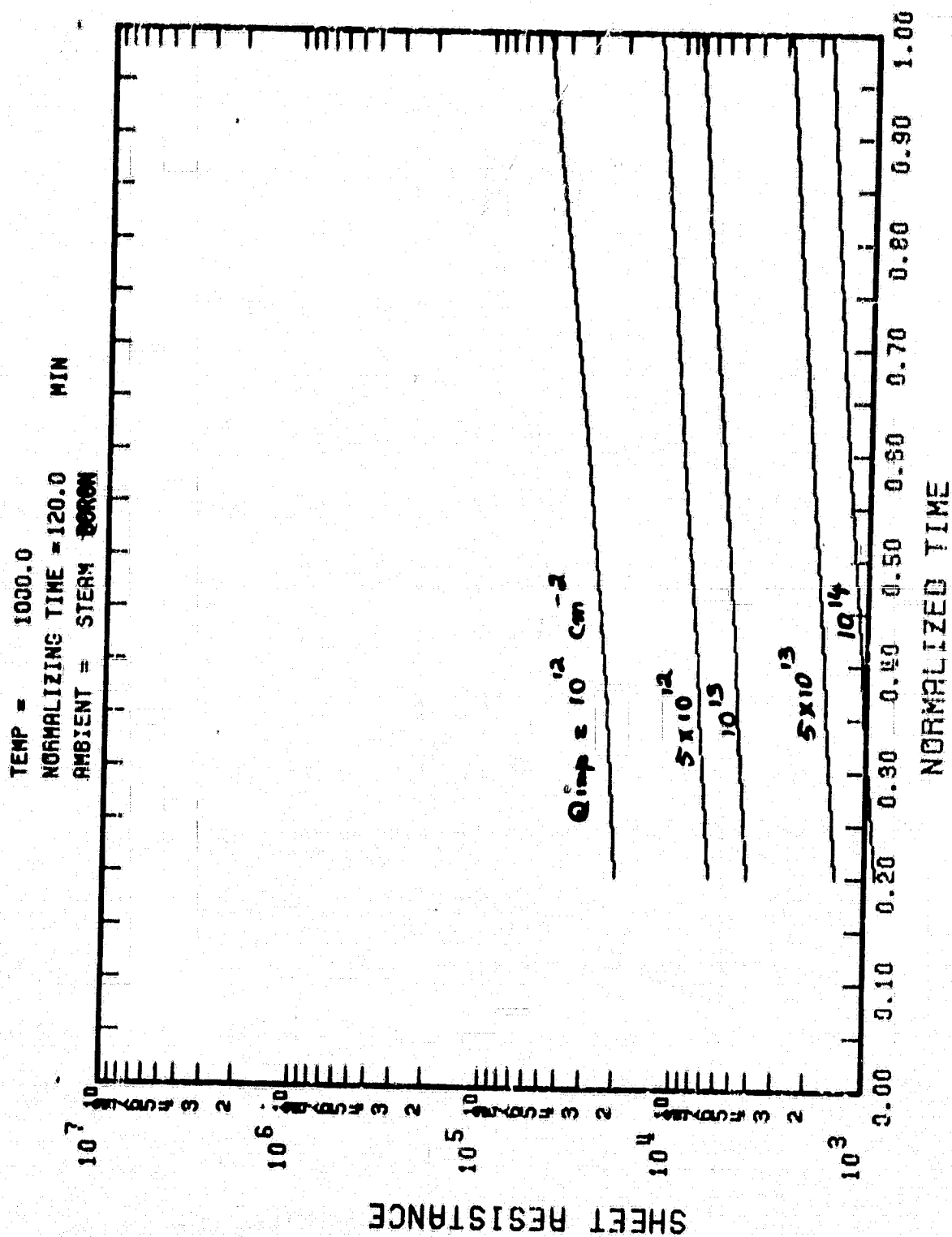


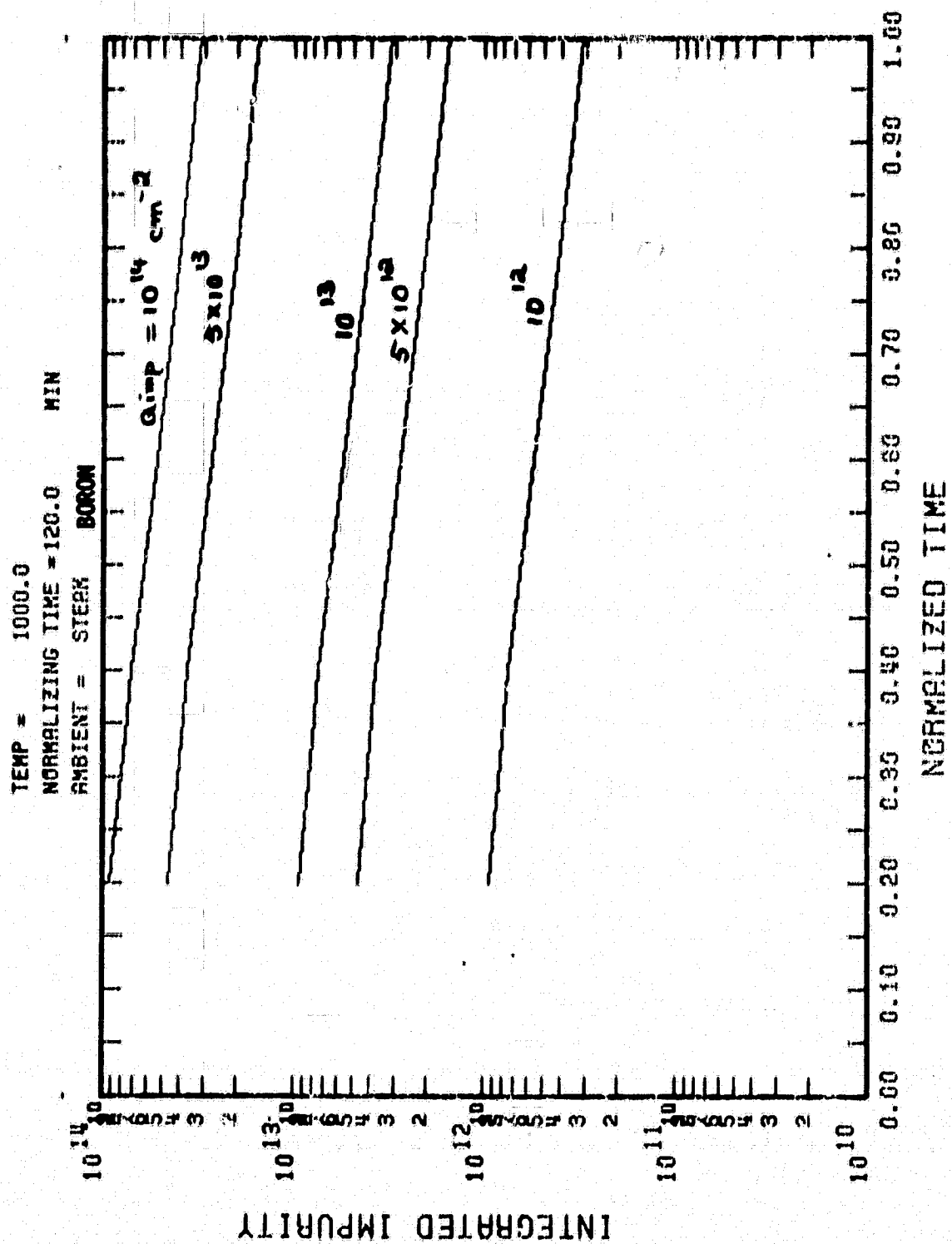
55

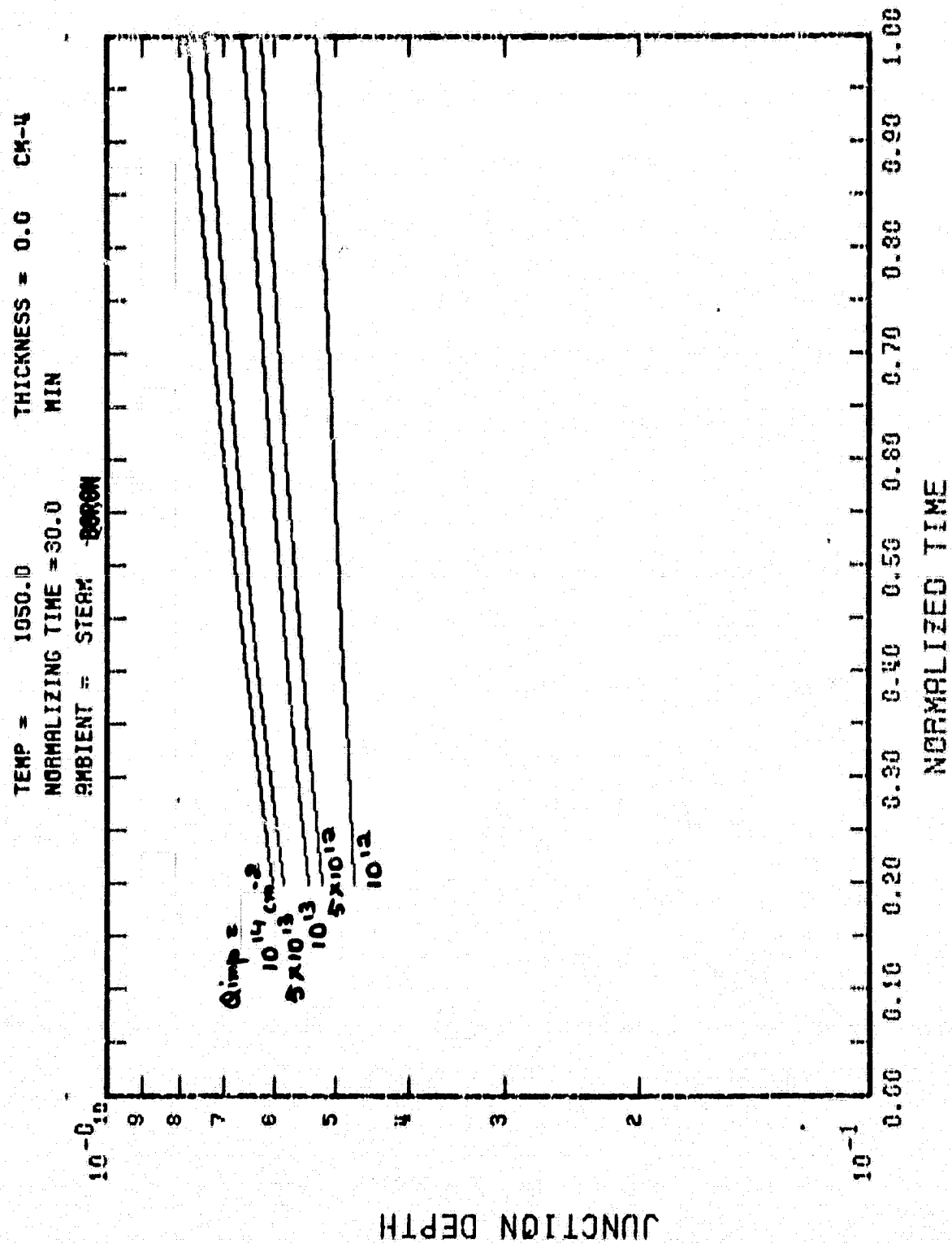




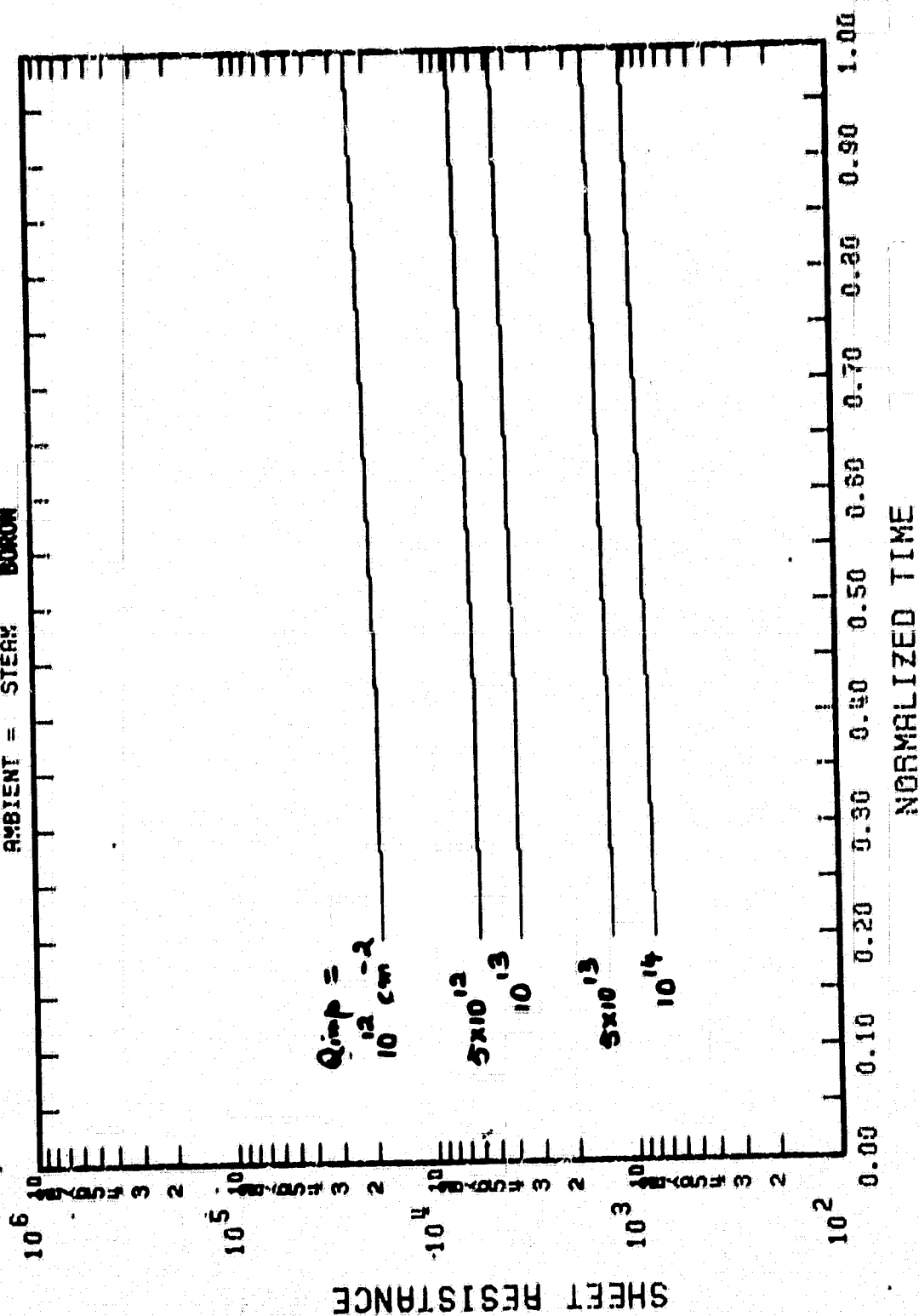
42



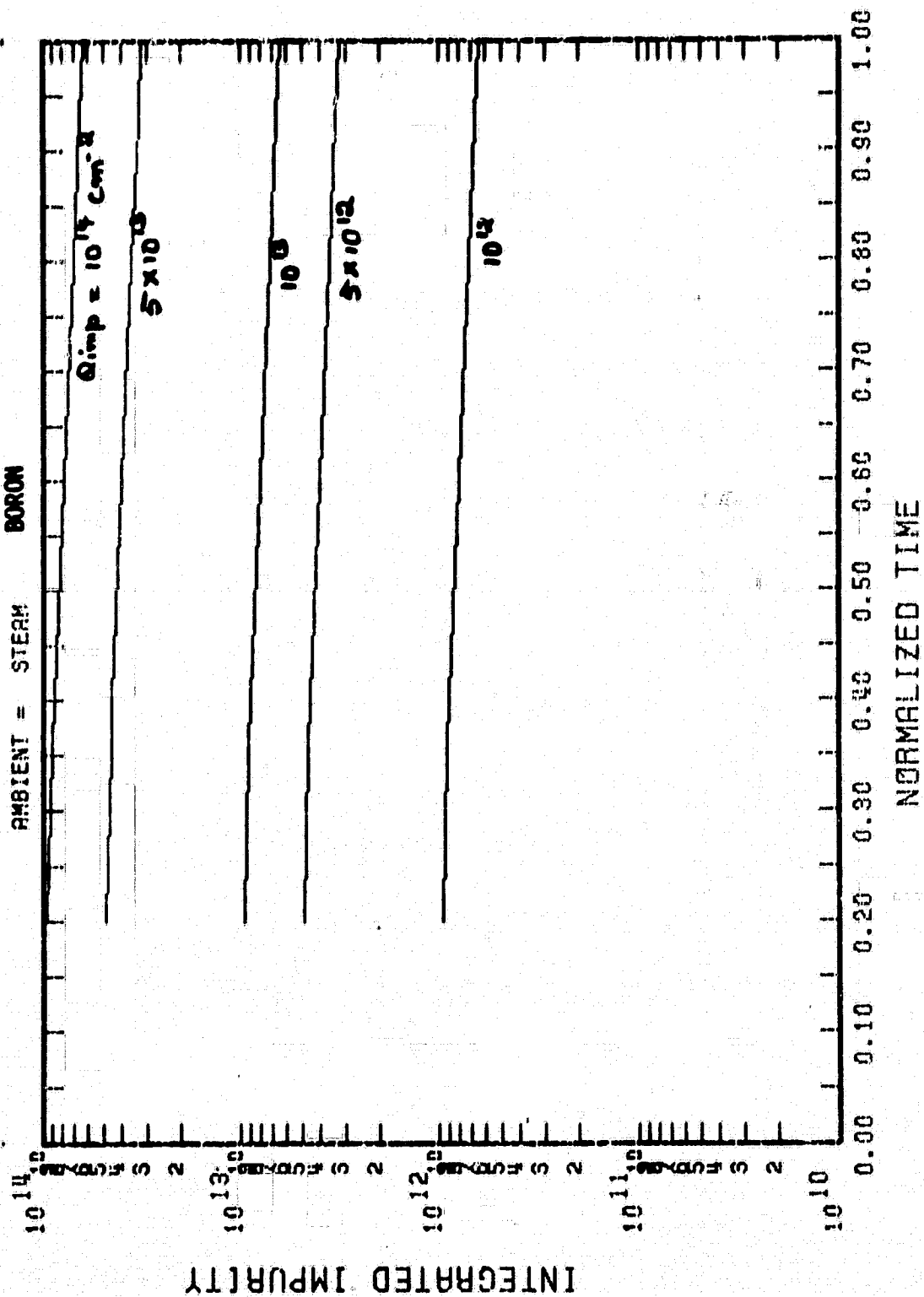




TEMP = 1050.0
 NORMALIZING TIME = 30.0 MIN
 AMBIENT = STEAK BORON



TEMP = 1050.0
 NORMALIZING TIME = 30.0 MIN
 AMBIENT = STEAM BORON

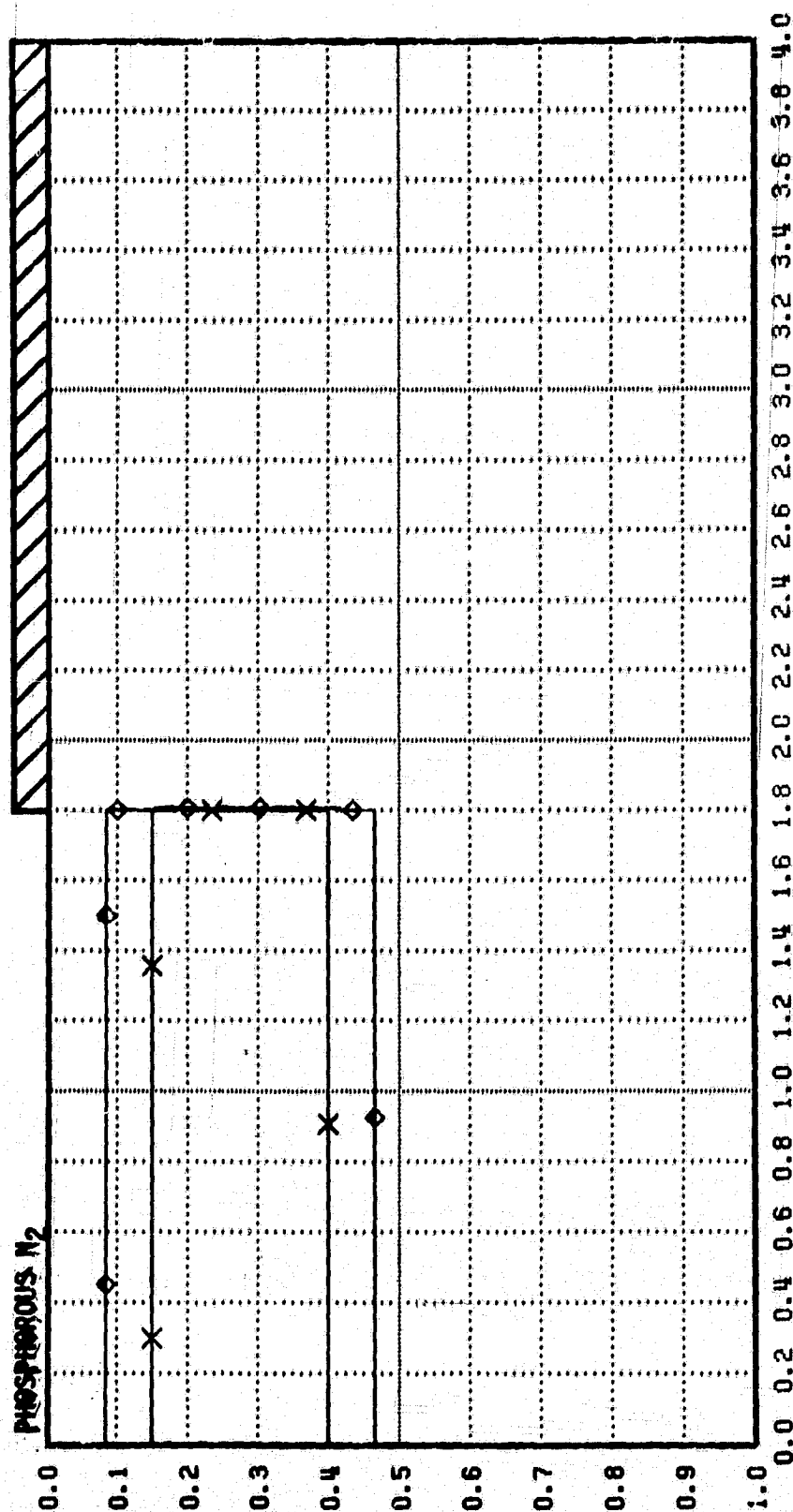


APPENDIX B

PHOSPHORUS DATA

λ^2 = 0.0308
 TEMPERATURE = 1000.
 TIME STEP = 0
 TIME = 0.00

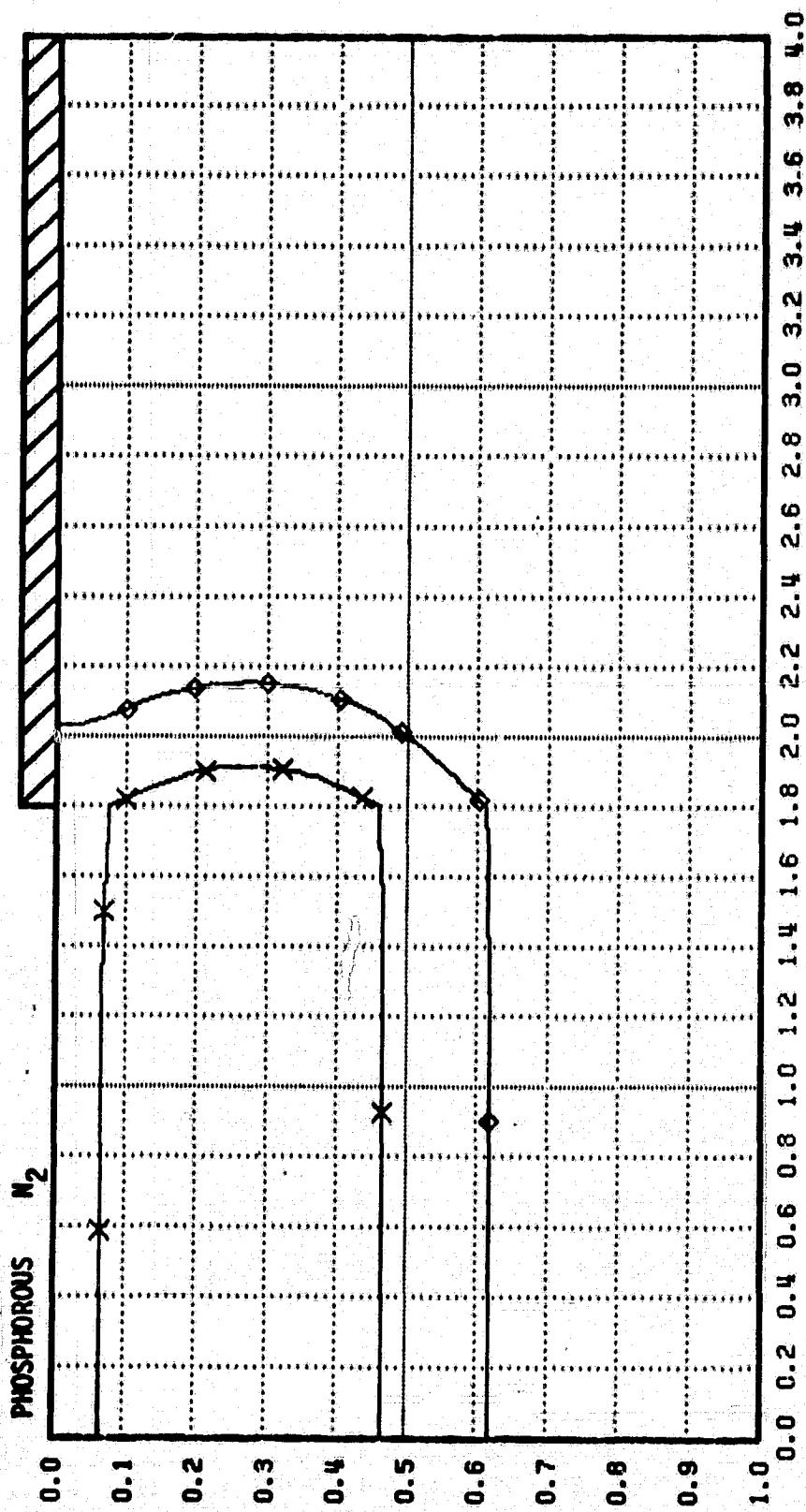
□ - 1.0E20
 ○ - 1.0E19
 ▲ - 1.0E18
 + - 1.0E17
 × - 1.0E16
 ◇ - 1.0E15



λ^2
 TEMPERATURE
 TIME STEP
 TIME

= 0.0308
 = 1000.
 = 10
 = 0.20

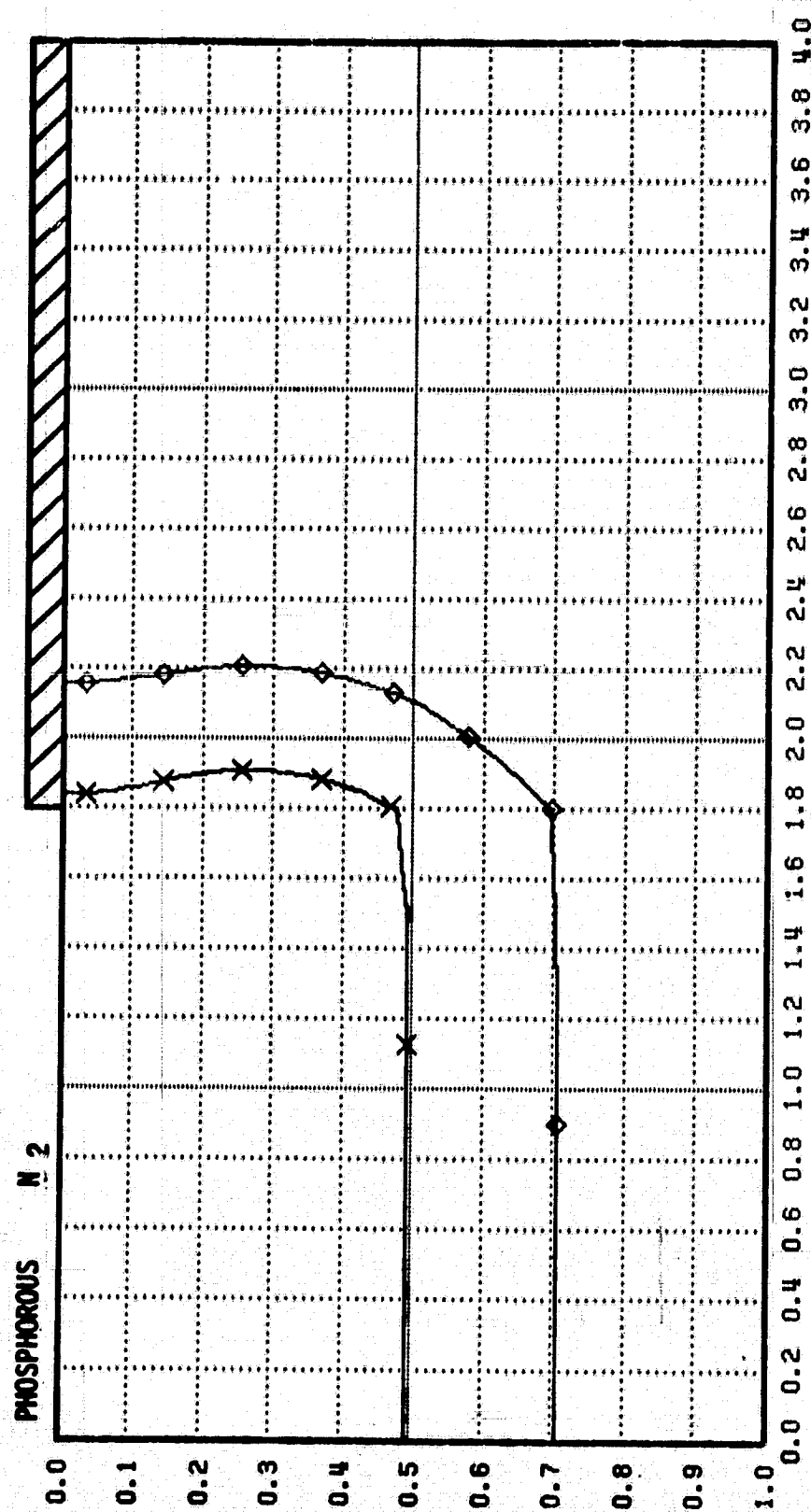
□ - 1.0E20
 ○ - 1.0E19
 ▲ - 1.0E18
 + - 1.0E17
 x - 1.0E16
 ◇ - 1.0E15



λ^2
 TEMPERATURE
 TIME STEP
 TIME

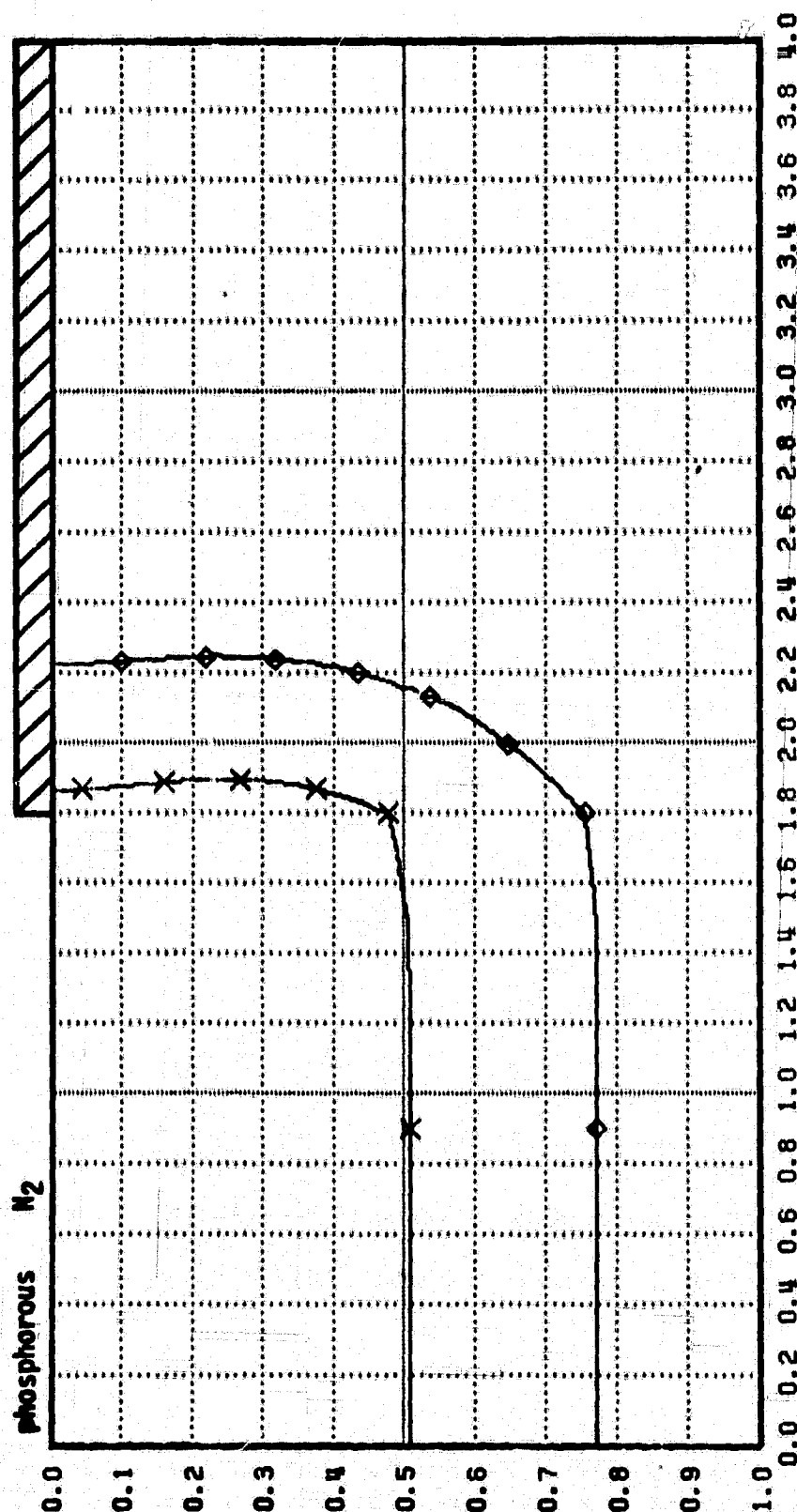
= 0.0308
 = 1000.
 = 20
 = 0.40

□ - 1.0E20
 ○ - 1.0E19
 △ - 1.0E18
 + - 1.0E17
 × - 1.0E16
 ◇ - 1.0E15



λ^2
 TEMPERATURE = 0.0308
 TIME STEP = 1000.
 TIME = 30
 = 0.60

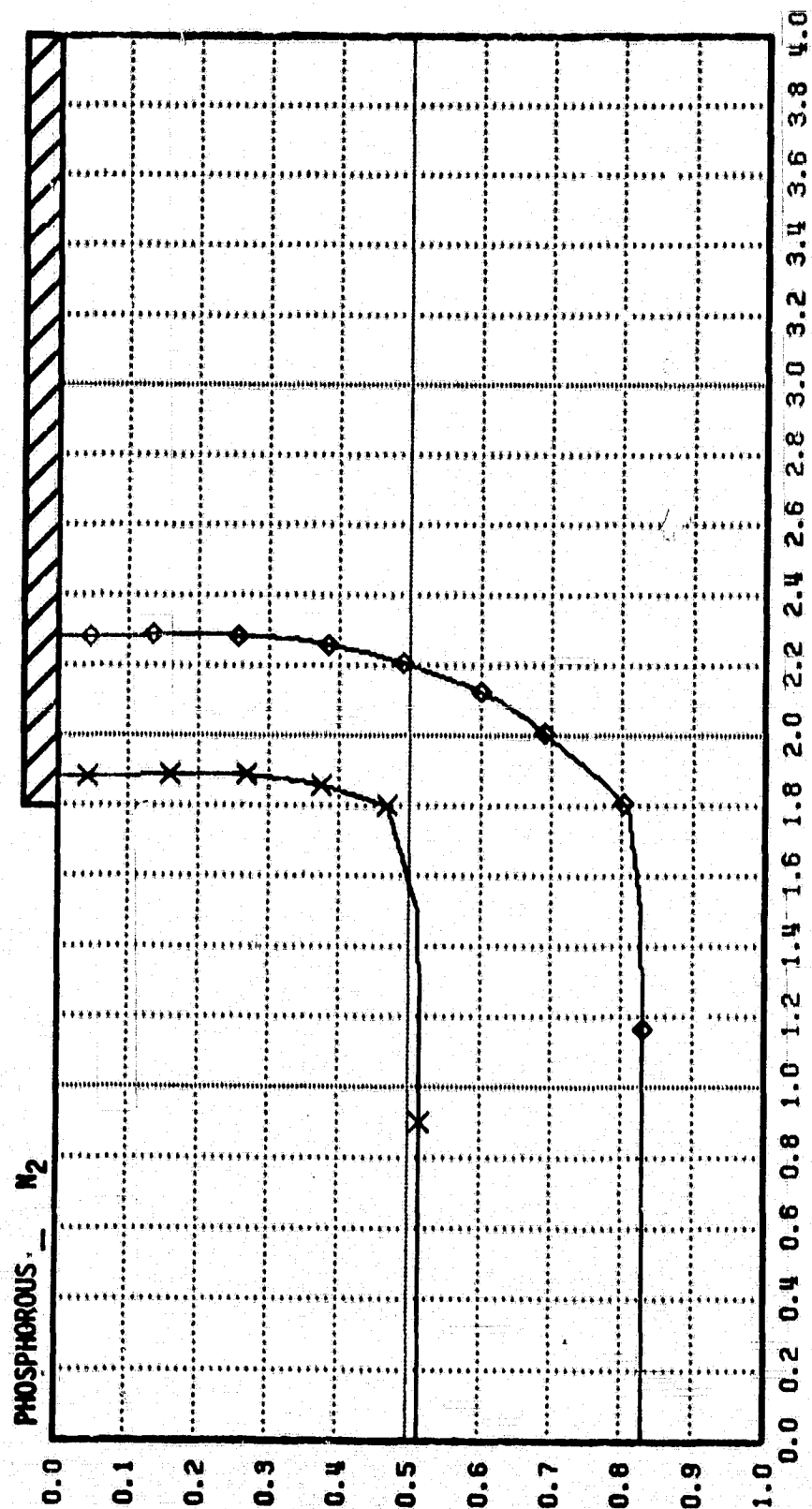
□ - 1.0E20
 ○ - 1.0E19
 △ - 1.0E18
 + - 1.0E17
 × - 1.0E16
 ◇ - 1.0E15



λ^2
 TEMPERATURE
 TIME STEP
 TIME

= 0.0308
 = 1000.
 = 40
 = 0.80

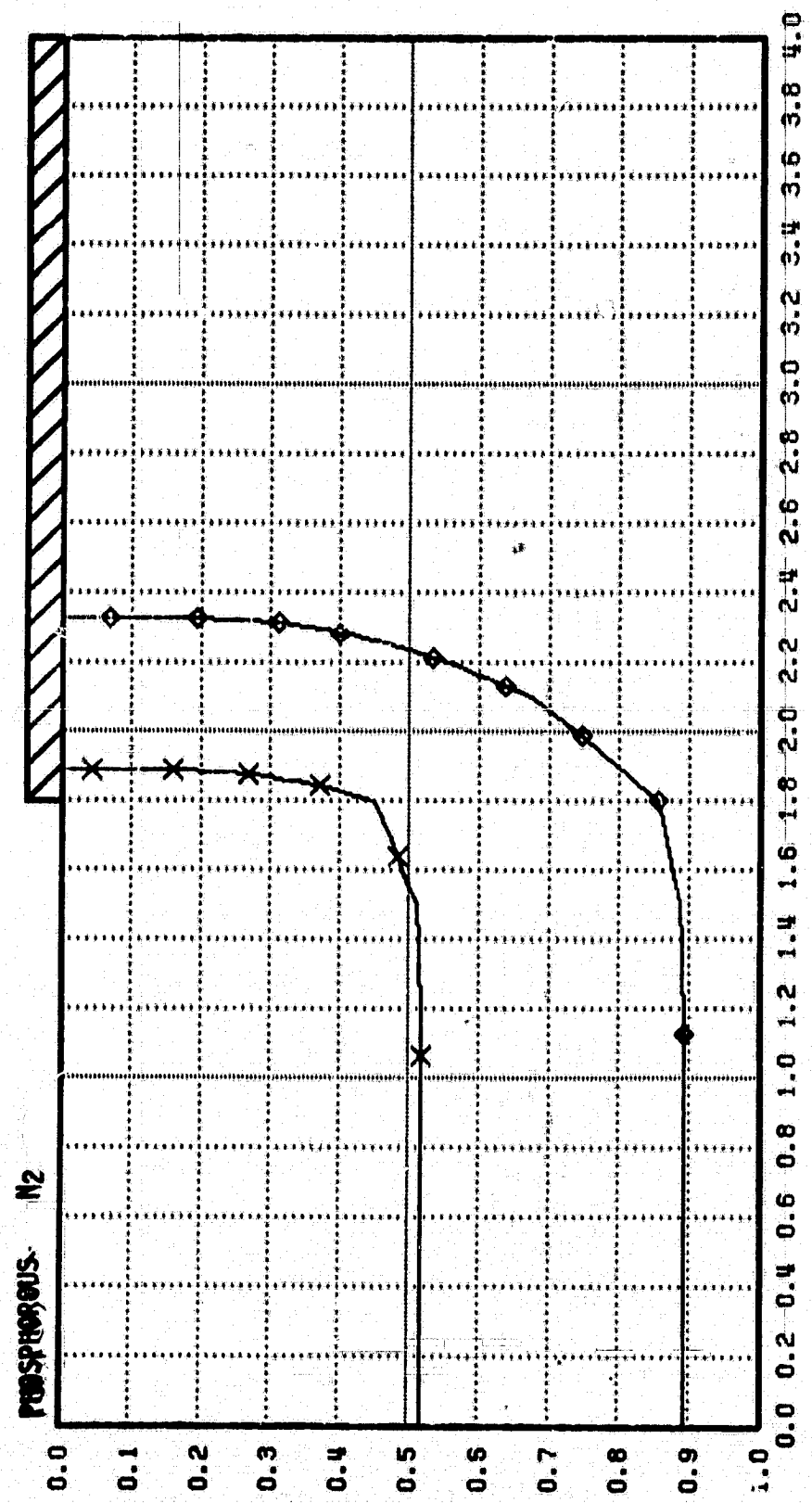
□ - 1.0E20
 ○ - 1.0E19
 △ - 1.0E18
 + - 1.0E17
 × - 1.0E16
 ◇ - 1.0E15



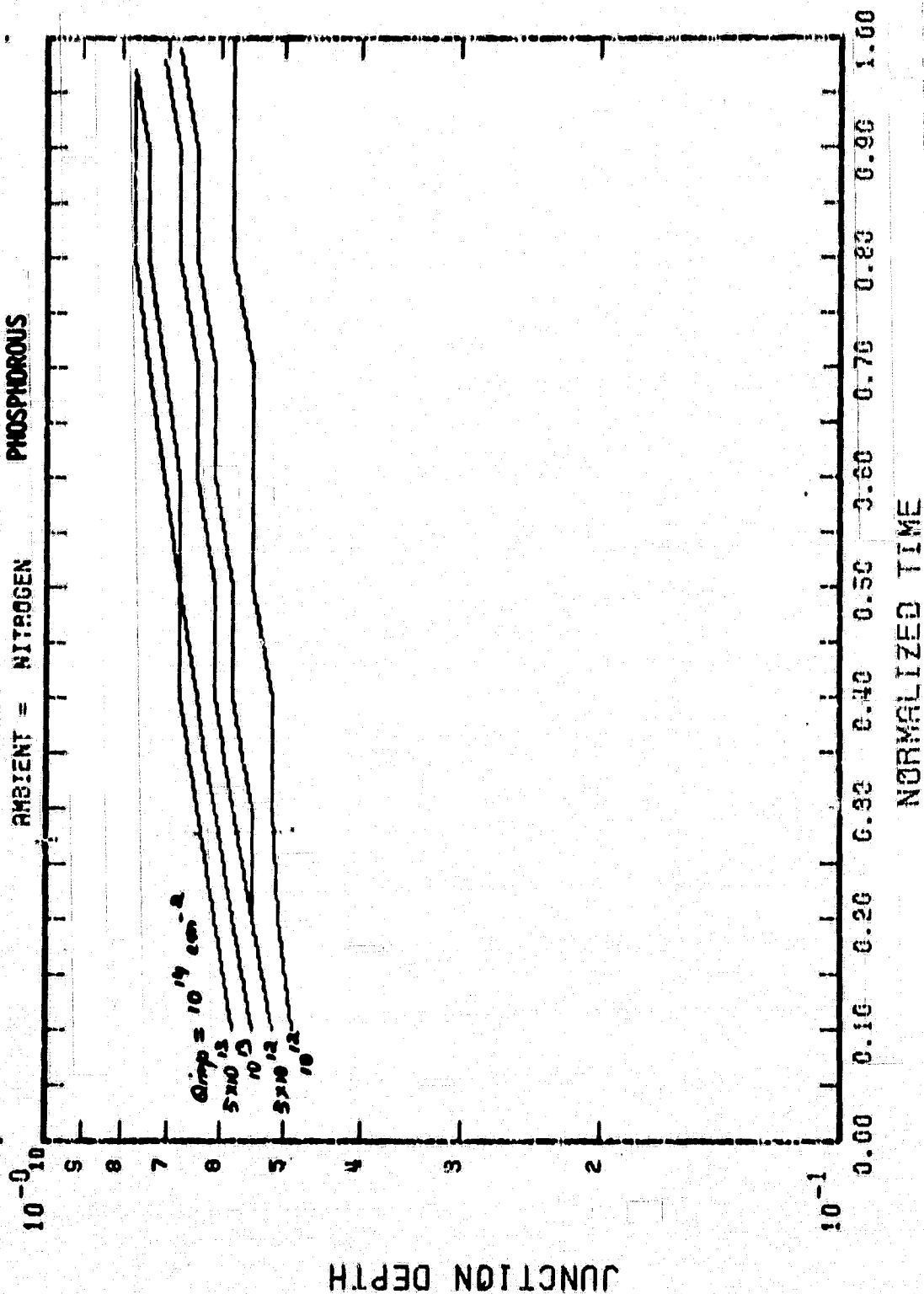
λ^2
 TEMPERATURE
 TIME STEP
 TIME

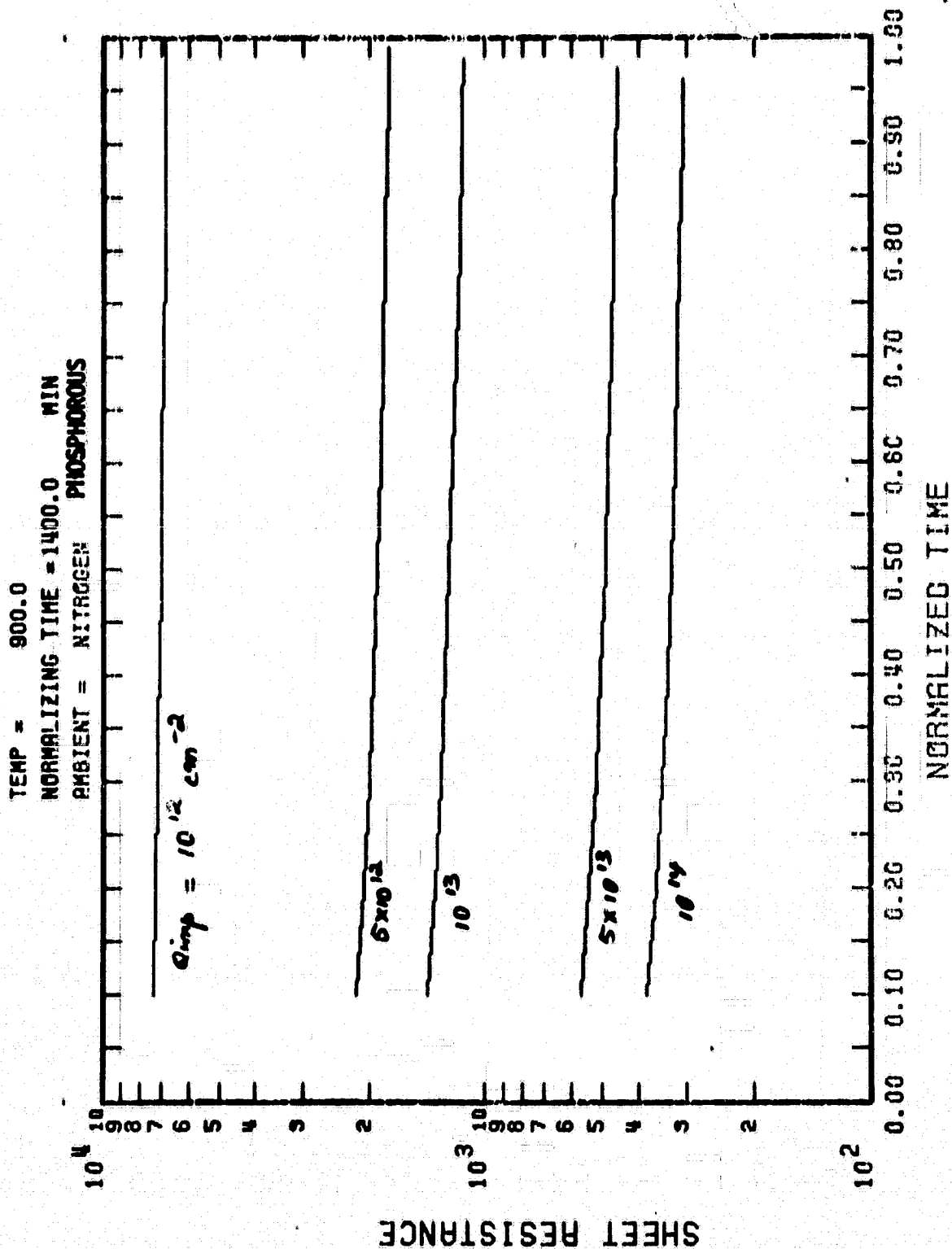
= 0.0308
 = 1000.
 = 50
 = 1.00

□ - 1.0E20
 ○ - 1.0E19
 ▲ - 1.0E18
 + - 1.0E17
 × - 1.0E16
 ◇ - 1.0E15

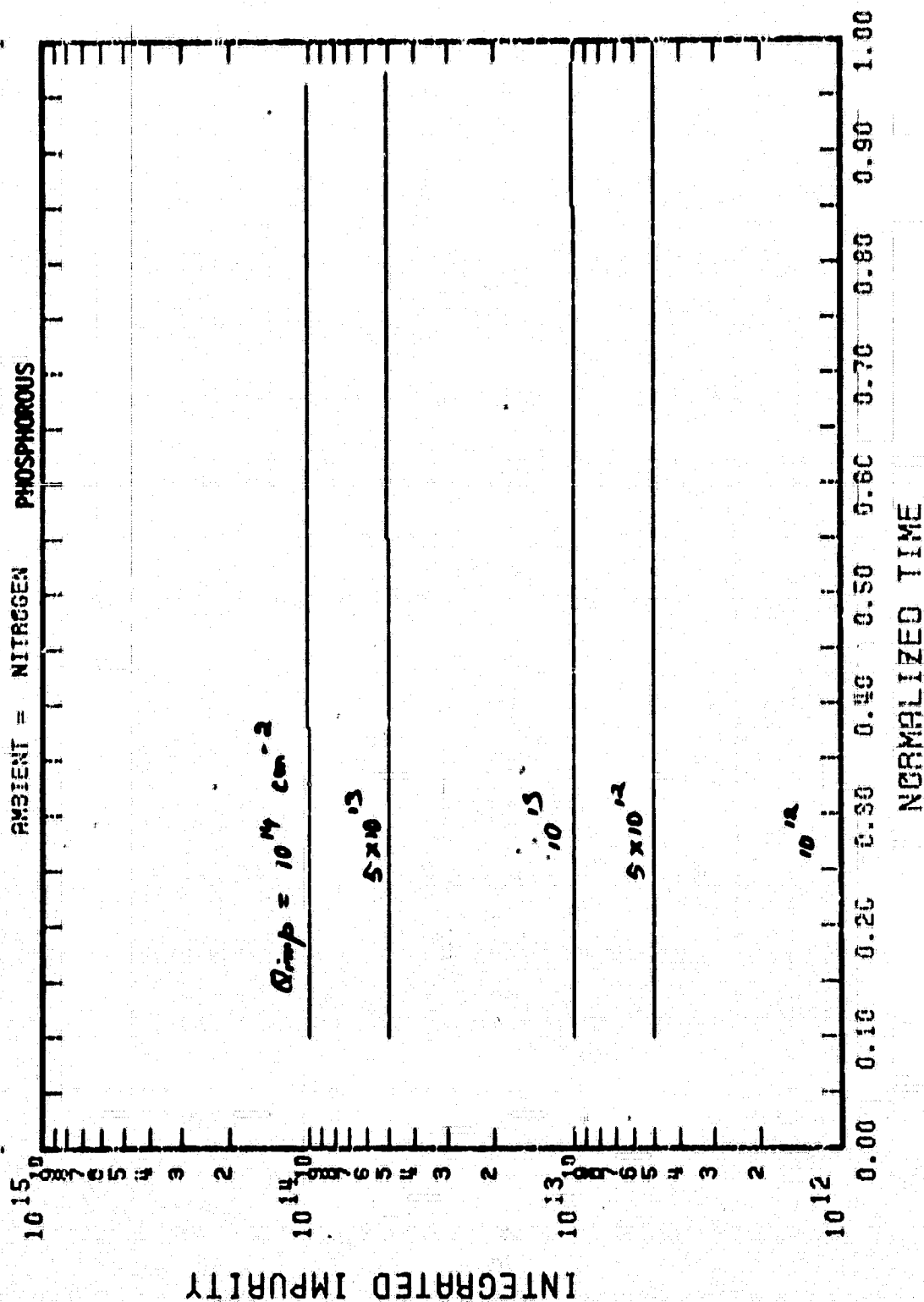


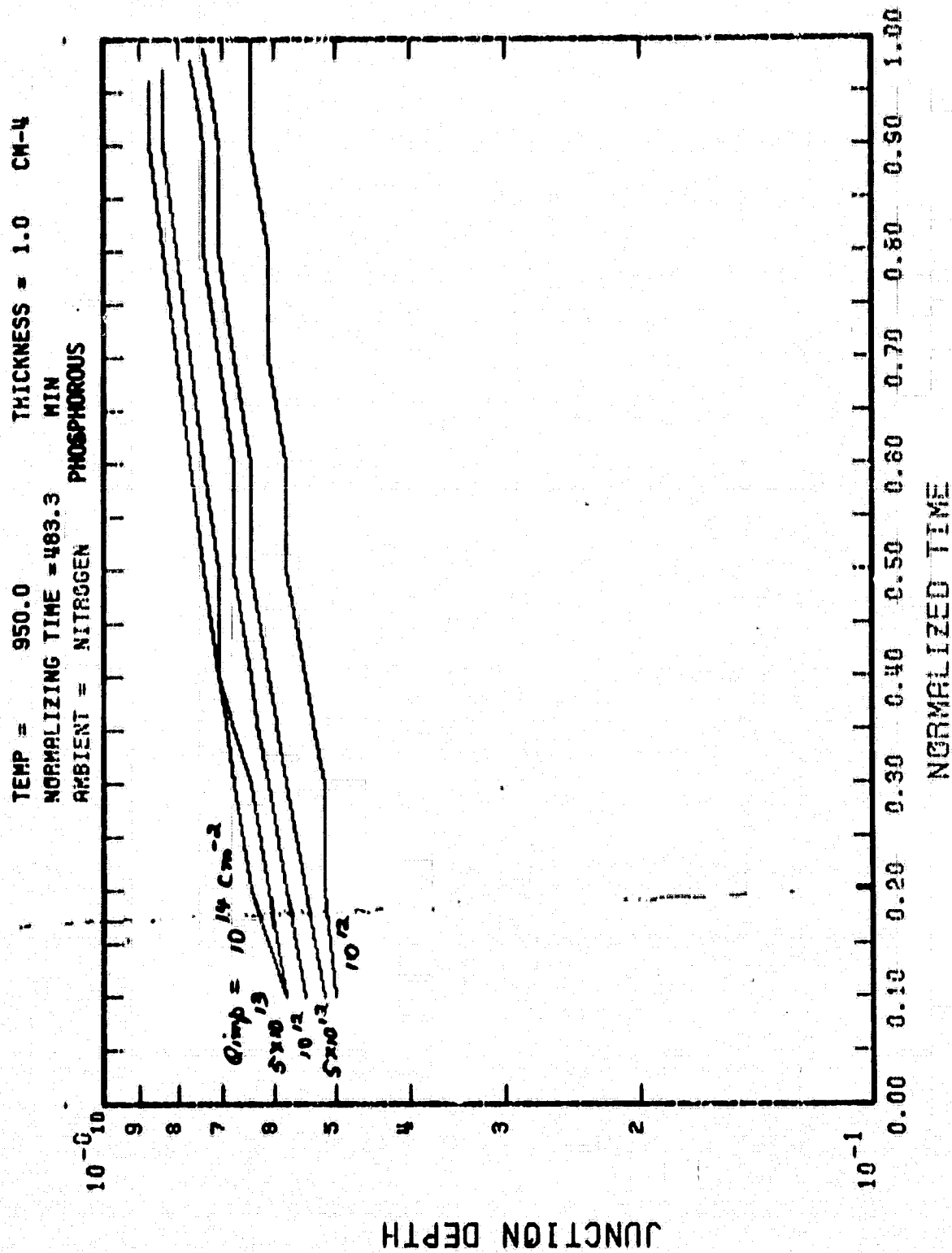
TEMP = 900.0 THICKNESS = 1.0 CM-4
 NORMALIZING TIME = 1400.0 MIN
 AMBIENT = NITROGEN PHOSPHOROUS





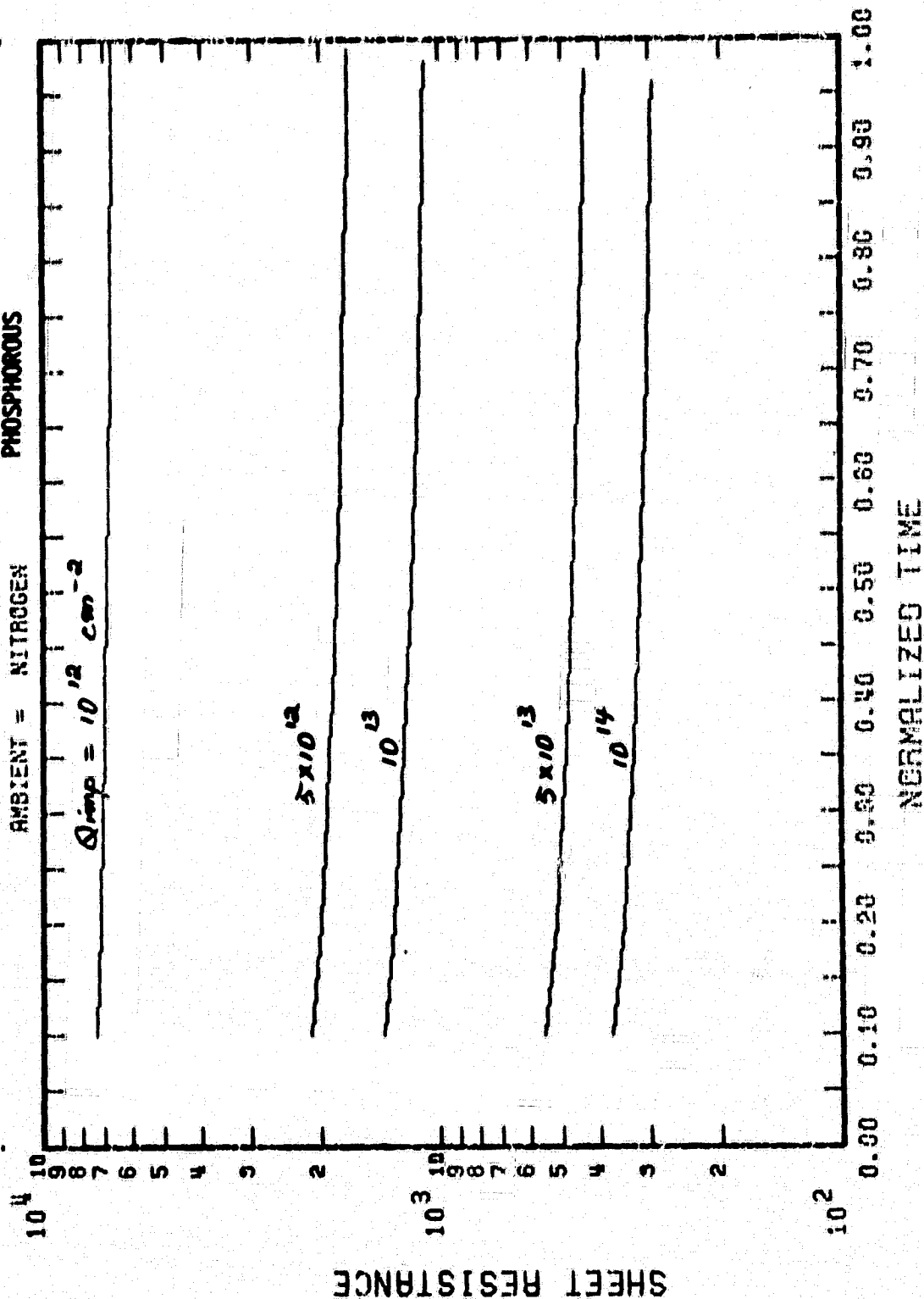
TEMP = 900.0
 NORMALIZING TIME = 1400.0 MIN
 AMBIENT = NITROGEN PHOSPHOROUS



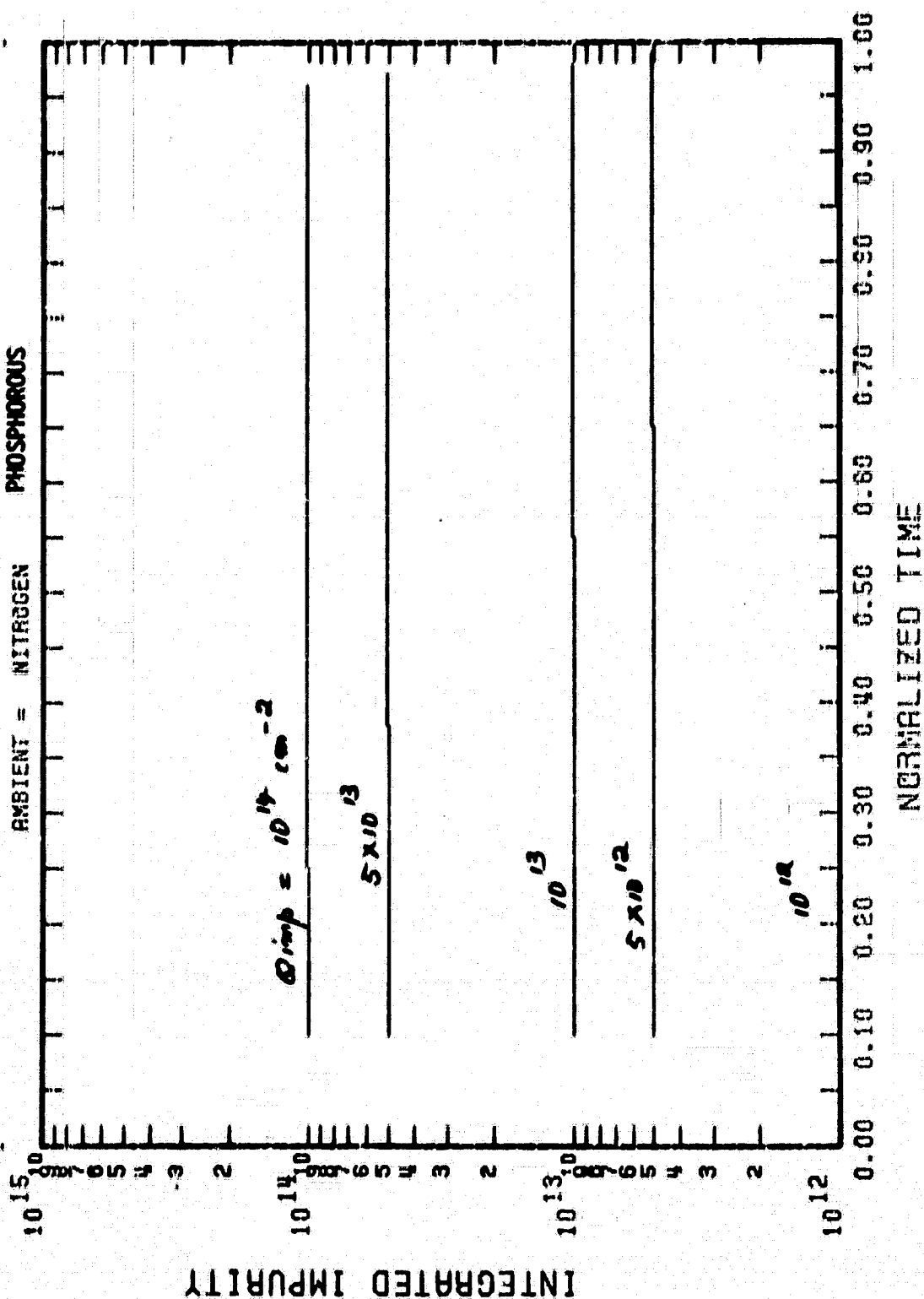


JUNCTION DEPTH

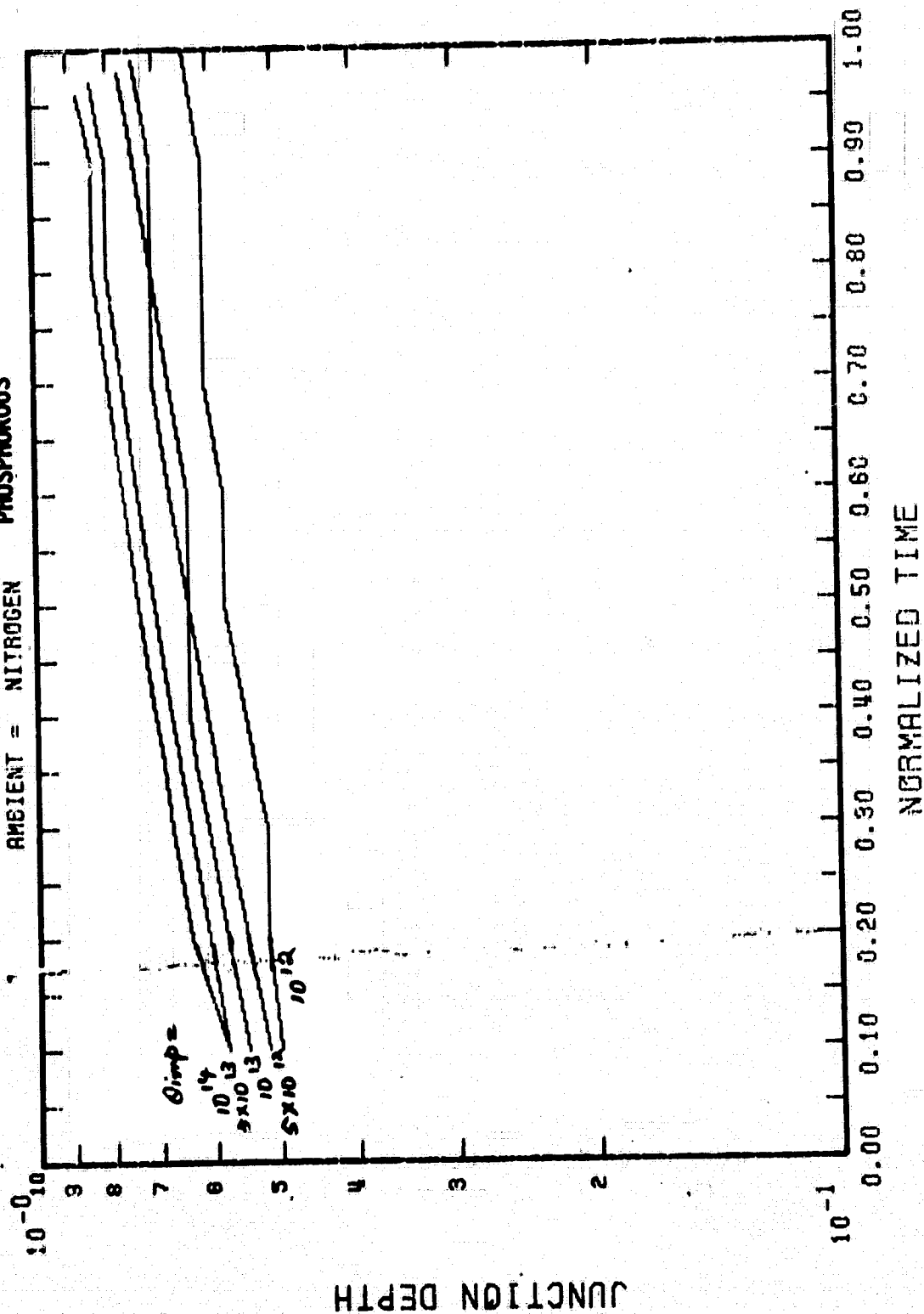
TEMP = 950.0
 NORMALIZING TIME = 483.3 MIN
 AMBIENT = NITROGEN PHOSPHOROUS



TEMP = 950.0
 NORMALIZING TIME = 483.3 MIN
 AMBIENT = NITROGEN PHOSPHOROUS

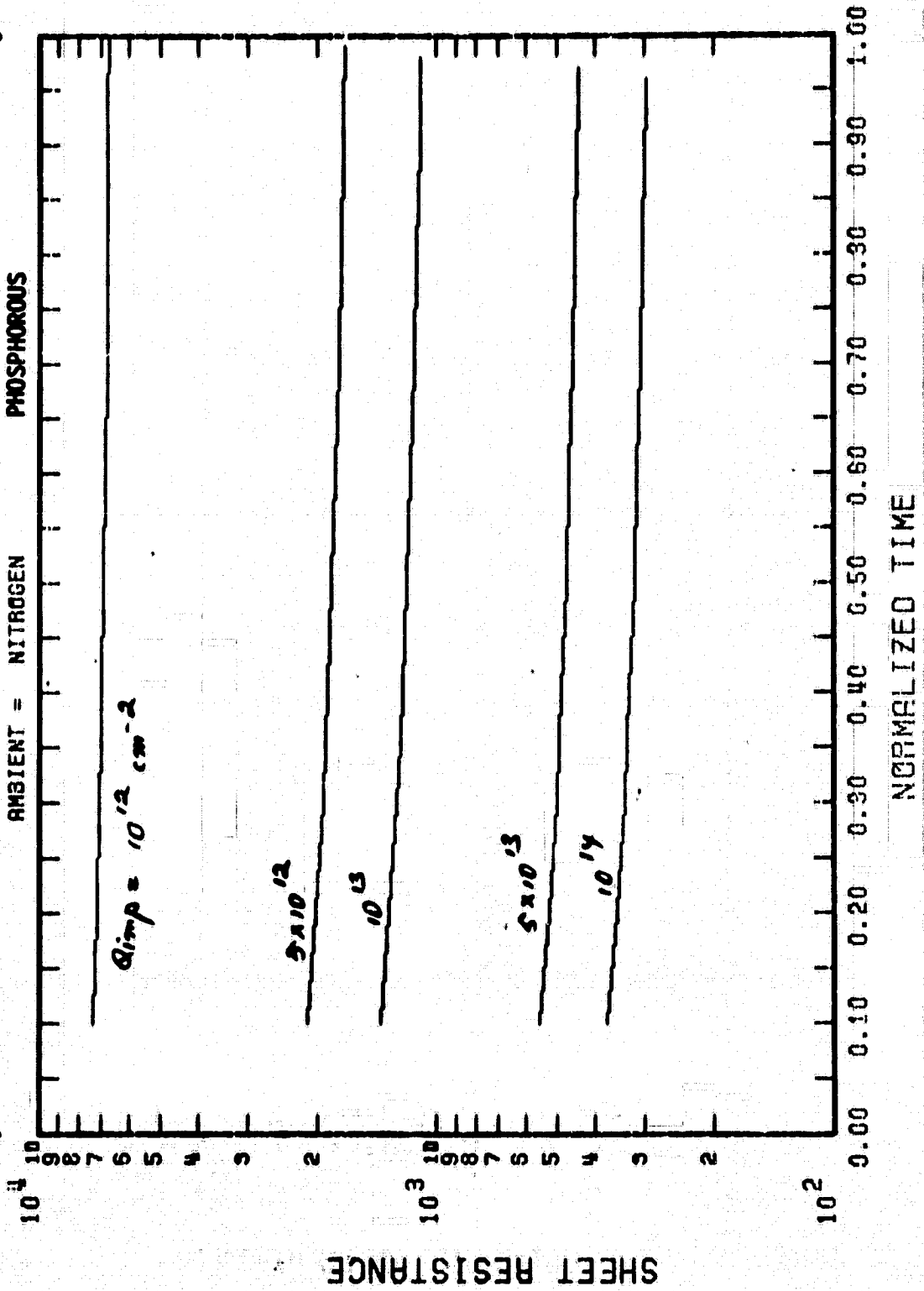


TEMP = 1000.0 THICKNESS = 1.0 CM-4
 NORMALIZING TIME = 120.0 MIN
 AMBIENT = NITROGEN PHOSPHOROUS

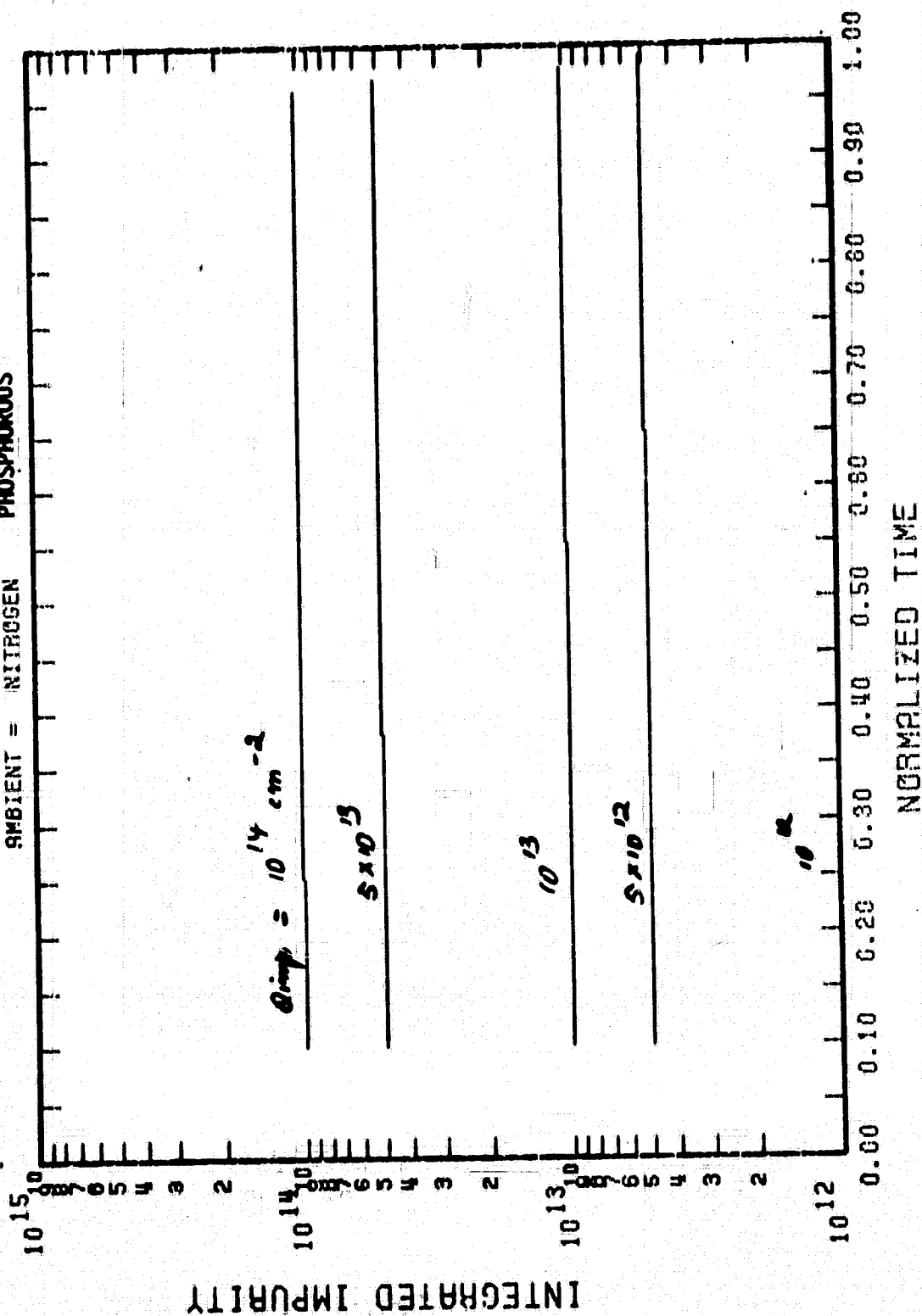


JUNCTION DEPTH

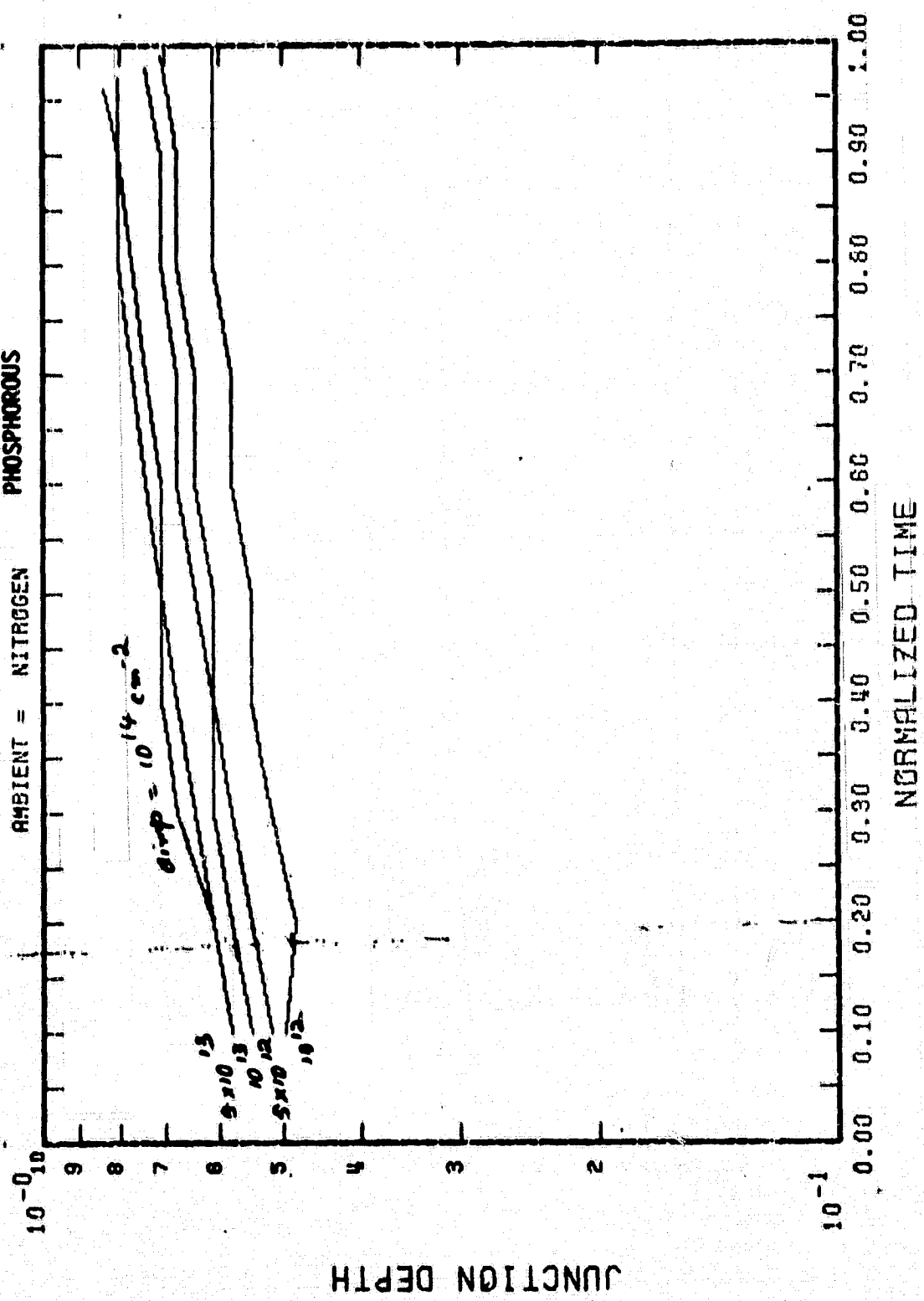
TEMP = 1000.0
NORMALIZING TIME = 120.0 MIN
AMBIENT = NITROGEN PHOSPHOROUS



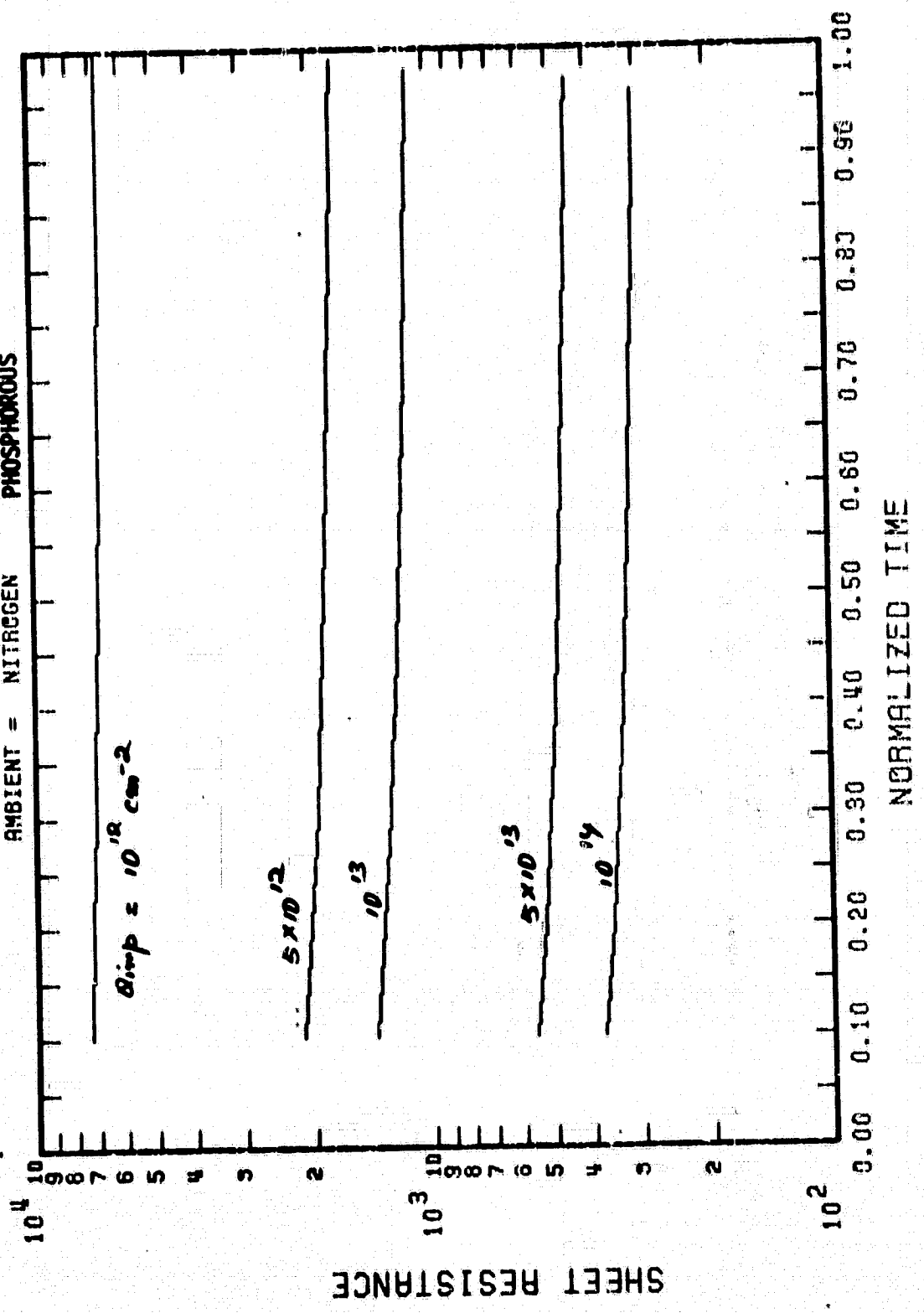
TEMP = 1000.0
 NORMALIZING TIME = 120.0 MIN
 AMBIENT = NITROGEN PHOSPHOROUS



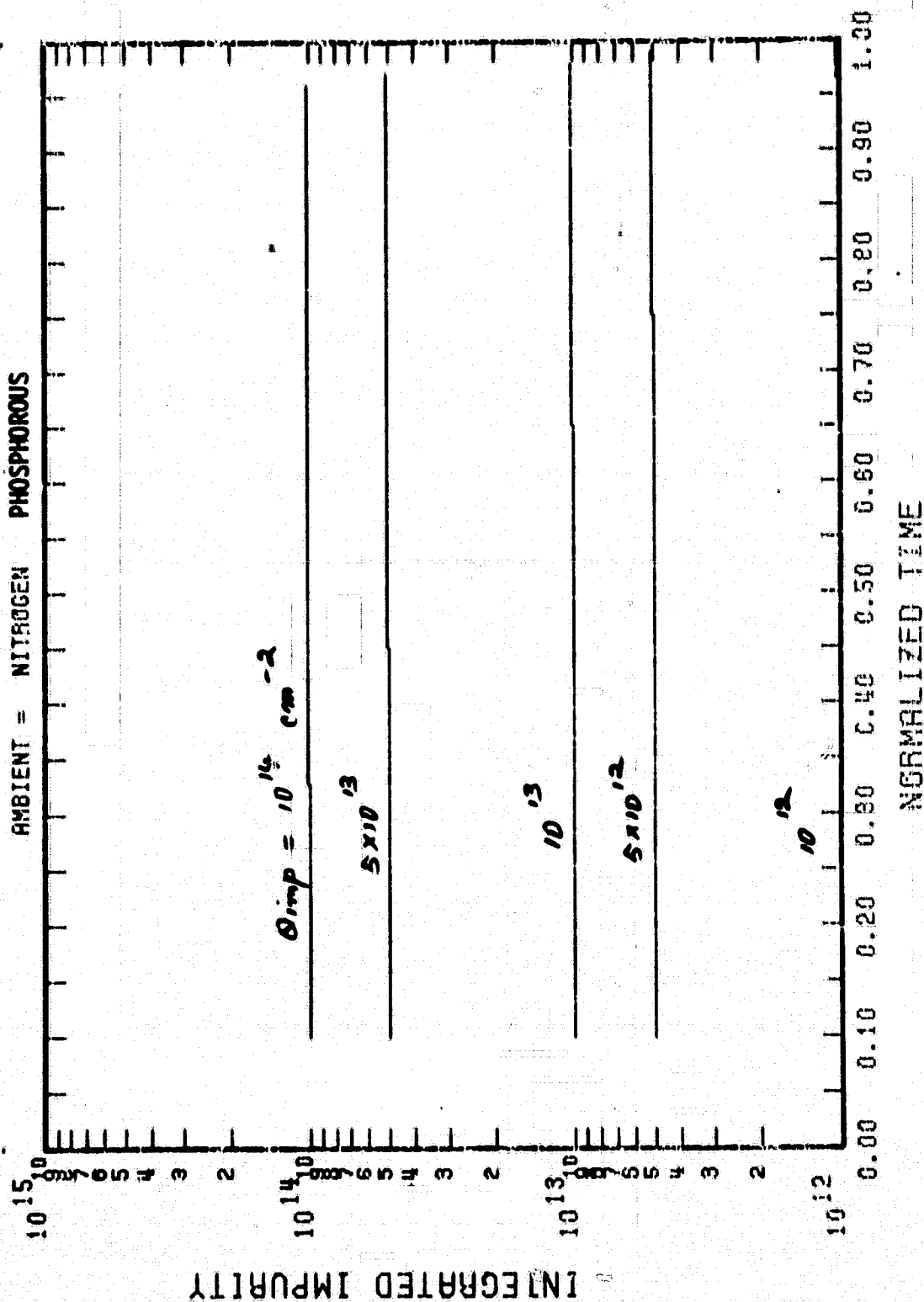
TEMP = 1050.0 THICKNESS = 1.0 CM-4
 NORMALIZING TIME = 30.0 MIN
 AMBIENT = NITROGEN PHOSPHOROUS



TEMP = 1050.0
NORMALIZING TIME = 30.0 MIN
AMBIENT = NITROGEN PHOSPHOROUS

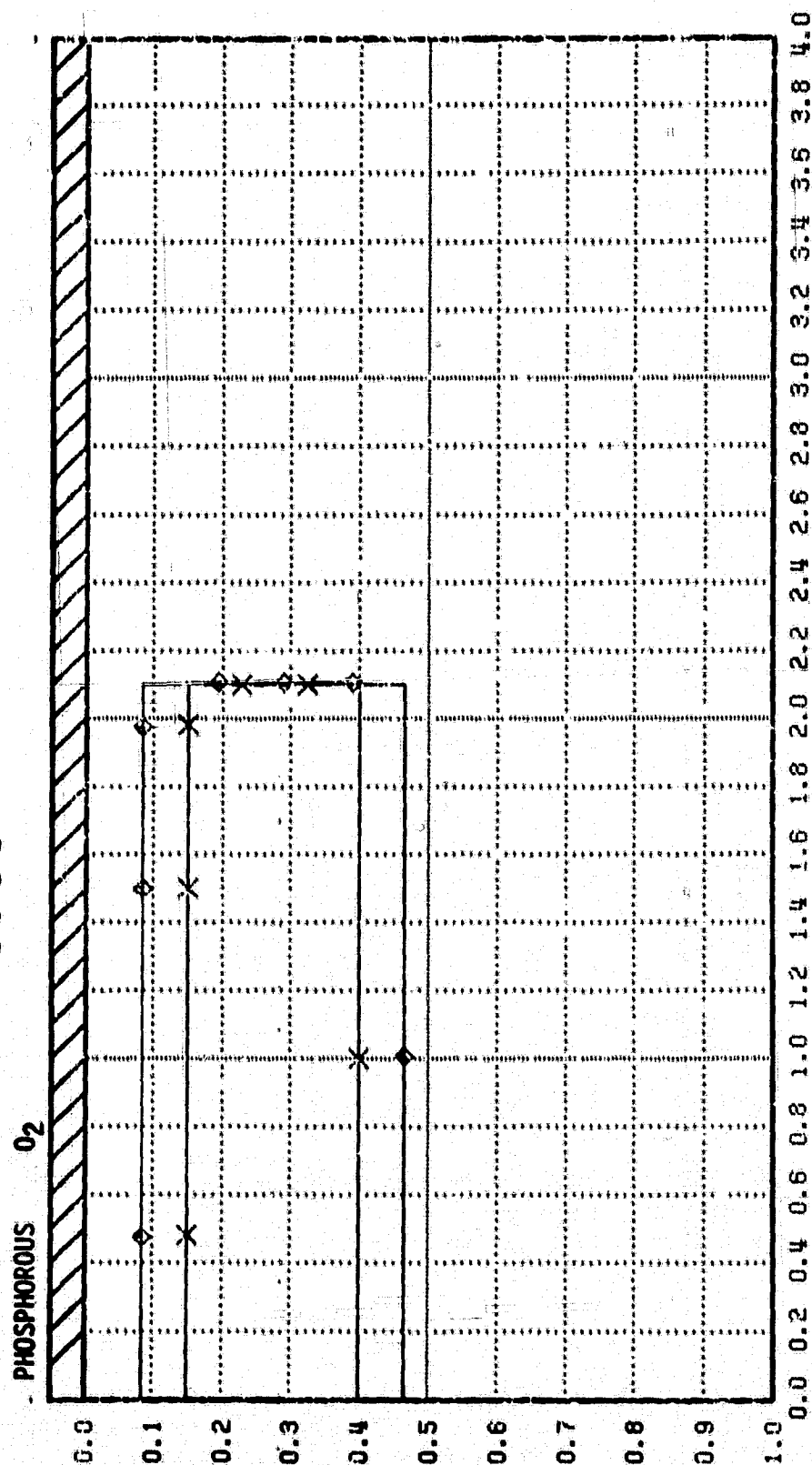


TEMP = 1050.0
 NORMALIZING TIME = 30.0 MIN
 AMBIENT = NITROGEN PHOSPHOROUS

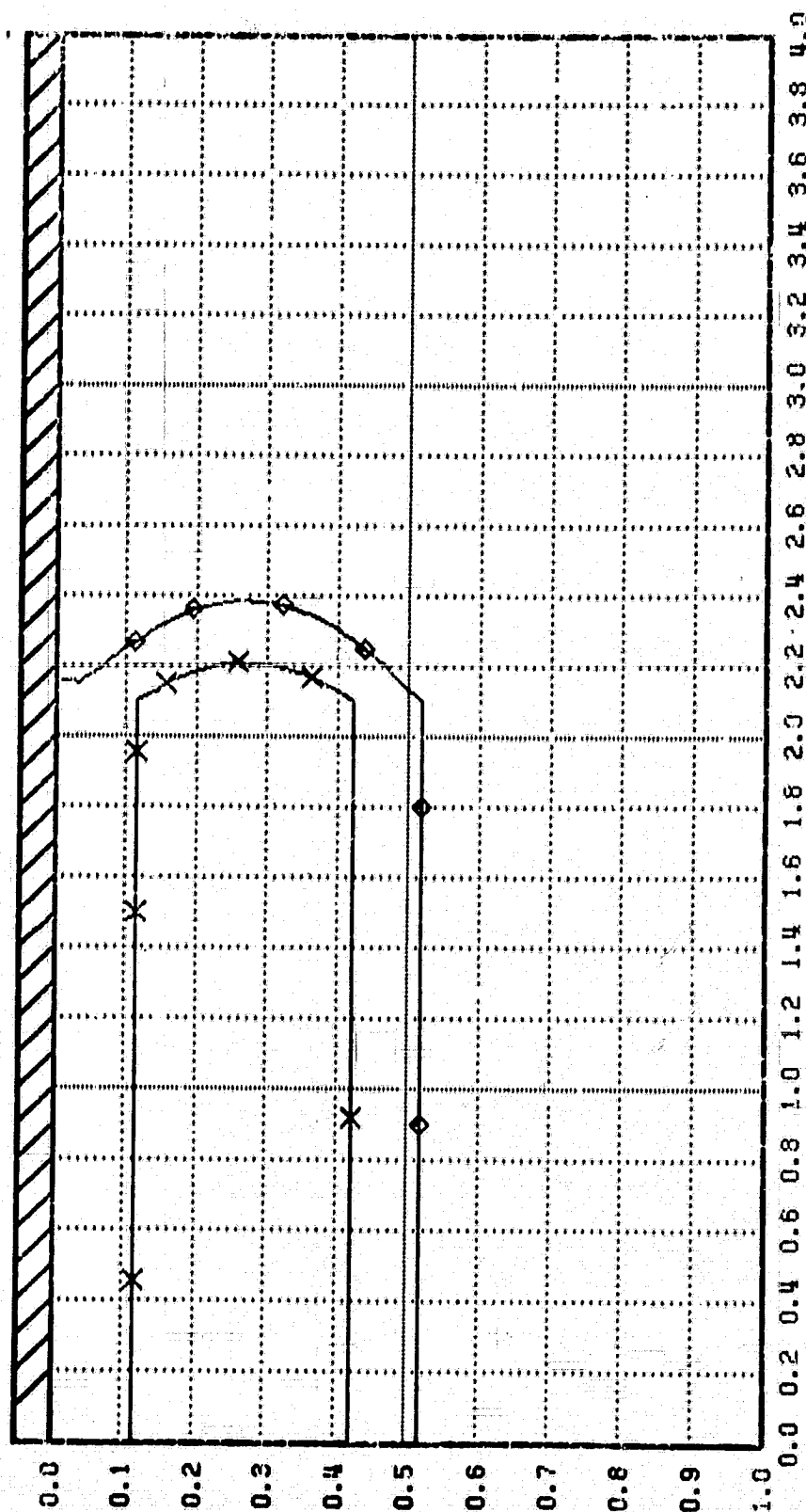


λ^2
 TEMPERATURE = 0.0000
 TIME STEP = 1000.
 TIME = 0
 TIME = 0.00

□ - 1.0E20
 ○ - 1.0E19
 △ - 1.0E18
 + - 1.0E17
 X - 1.0E16
 ◇ - 1.0E15

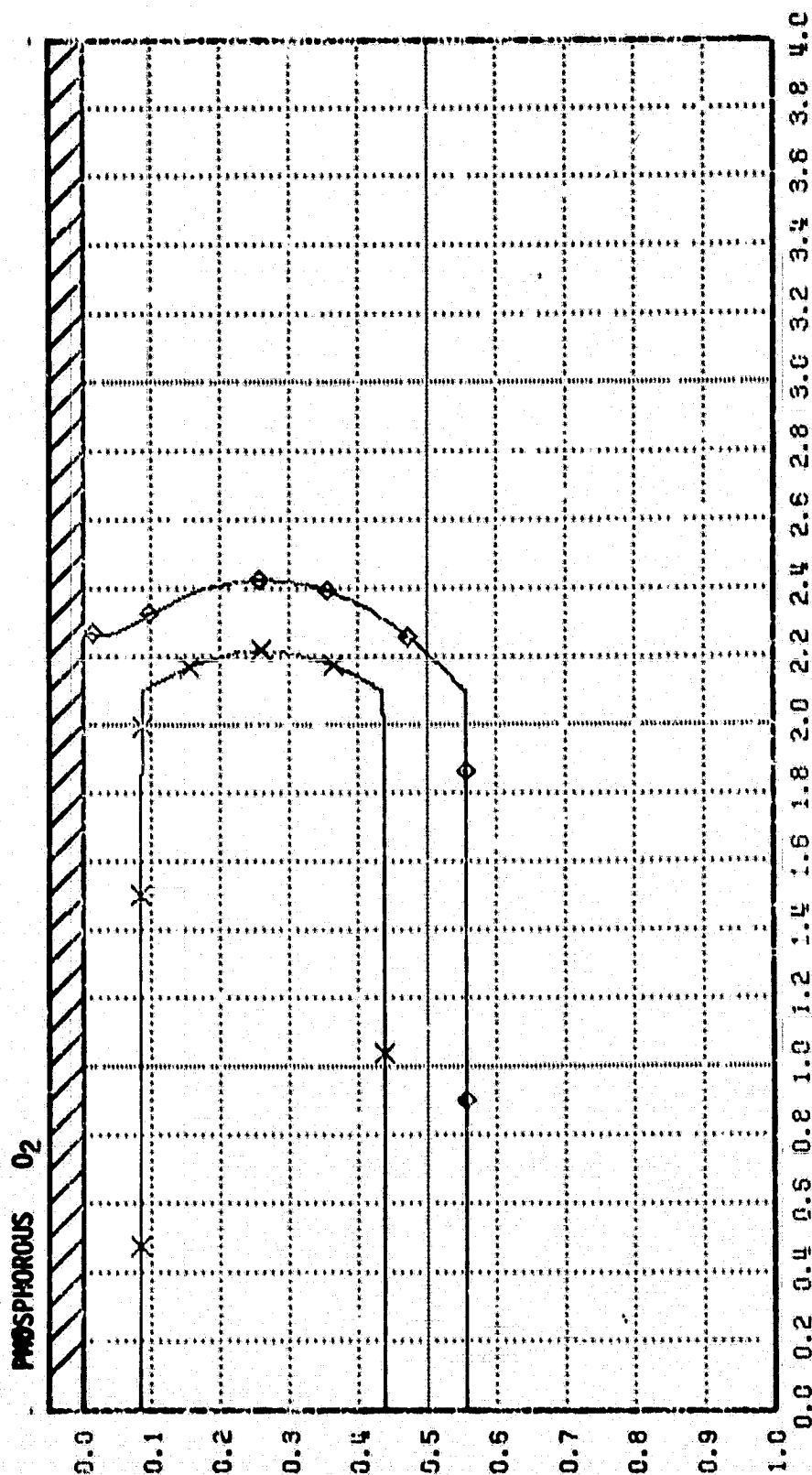


λ^2
 TEMPERATURE = 0.0000
 TIME STEP = 1000.
 TIME = 20
 TIME PHOSPHOROUS O₂ = 1440.00



λ^2
 TEMPERATURE = 0.0000
 TIME STEP = 1000.
 TIME = 40
 TIME = 2880.00

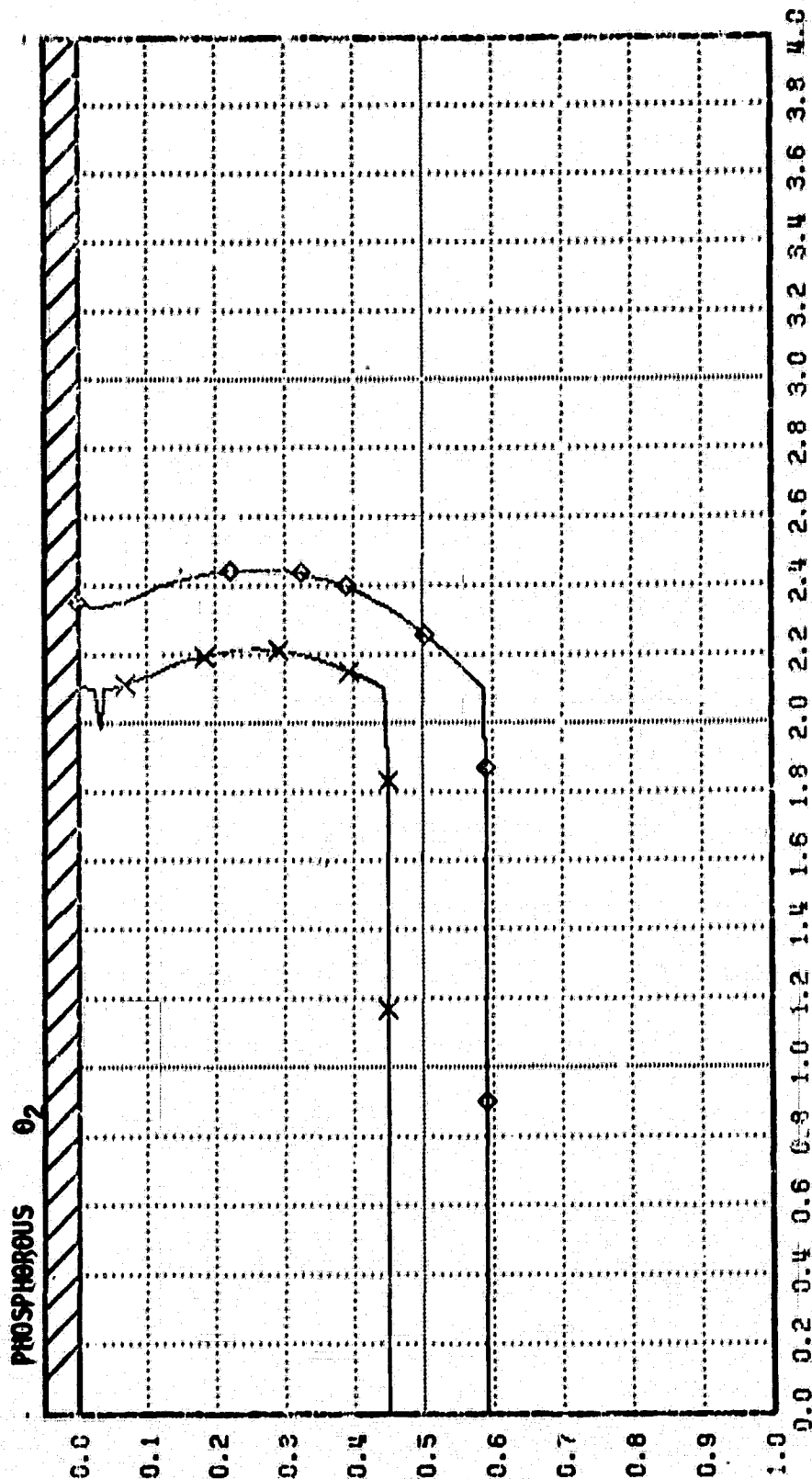
E - 1.0E20
 O - 1.0E19
 A - 1.0E18
 + - 1.0E17
 X - 1.0E16
 D - 1.0E15



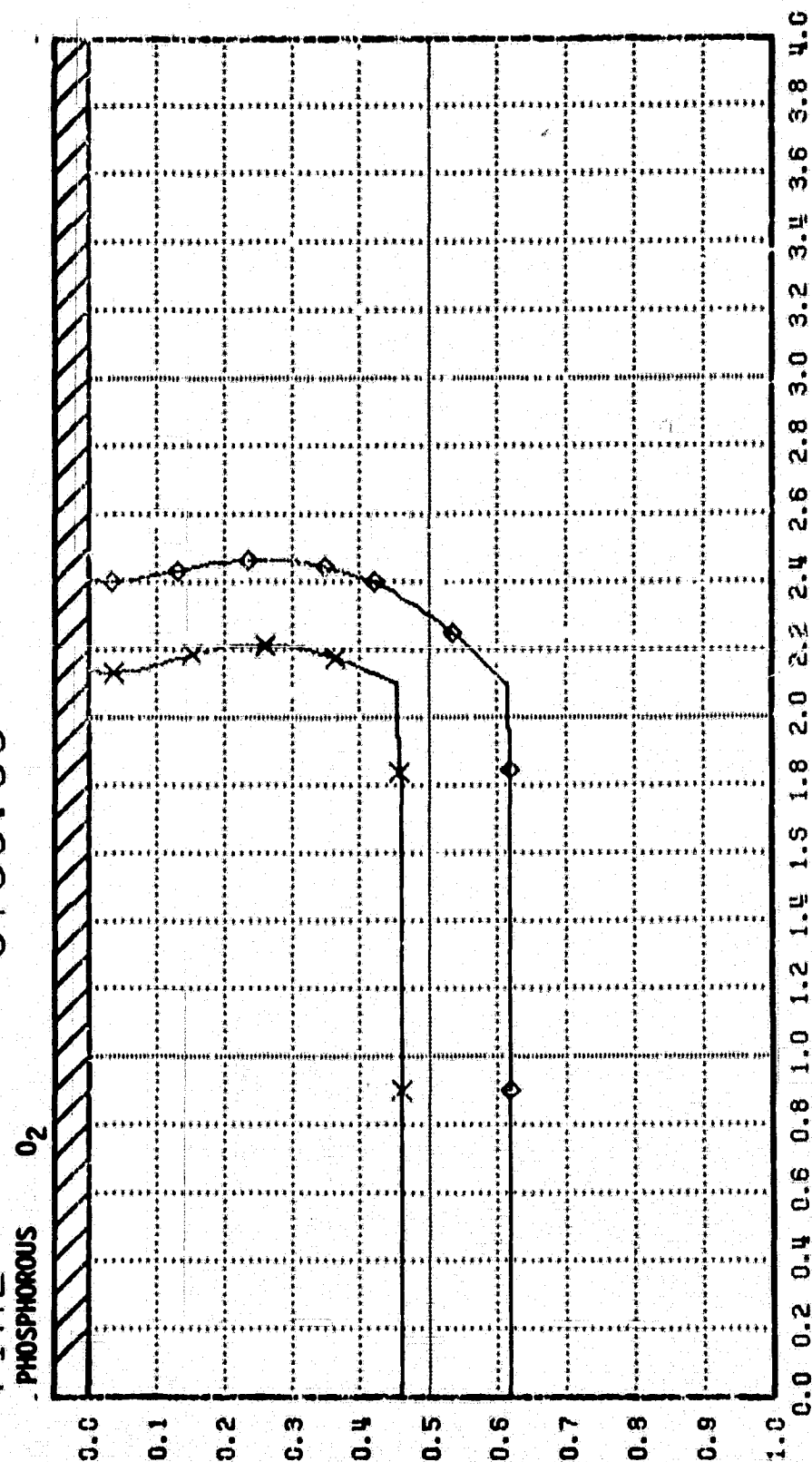
λ^2
 TEMPERATURE
 TIME STEP
 TIME

= 0.0000
 = 1000.
 = 60
 = 4320.00

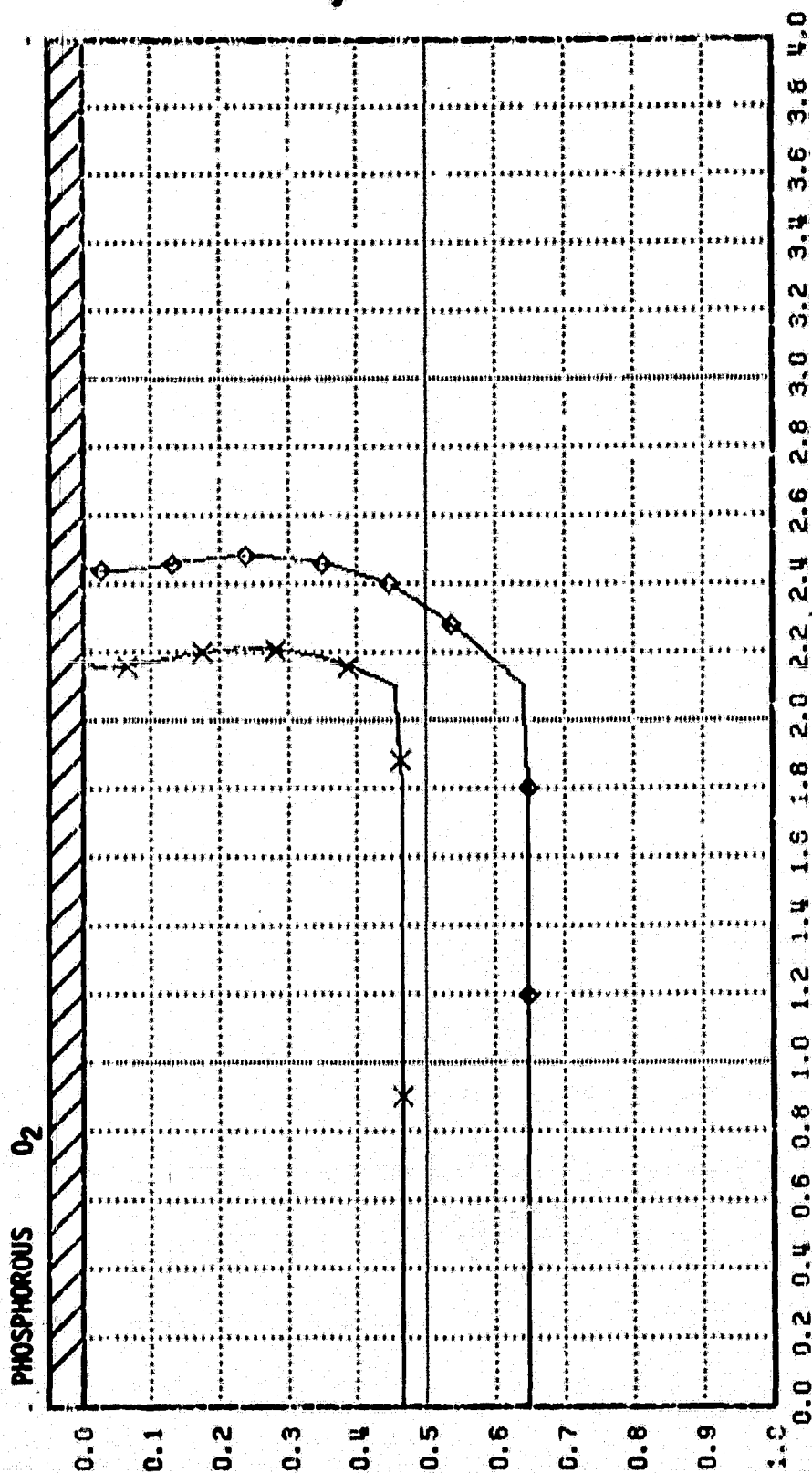
- 1.0E20
 - 1.0E19
 - 1.0E18
 - 1.0E17
 - 1.0E16
 - 1.0E15

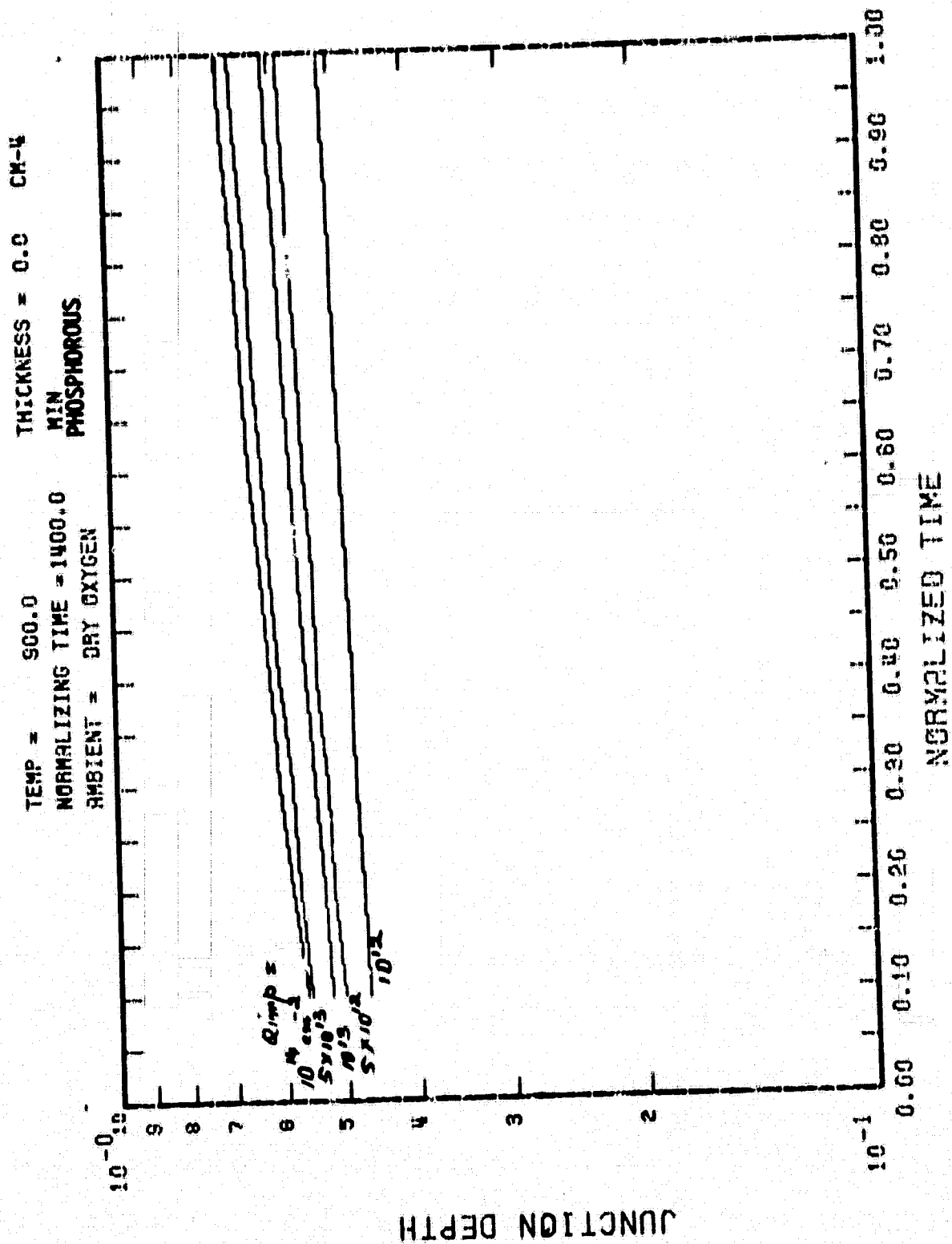


λ^2
 TEMPERATURE = 0.0000
 TIME STEP = 1000.
 TIME = 80
 PHOSPHOROUS O₂ = 5760.00

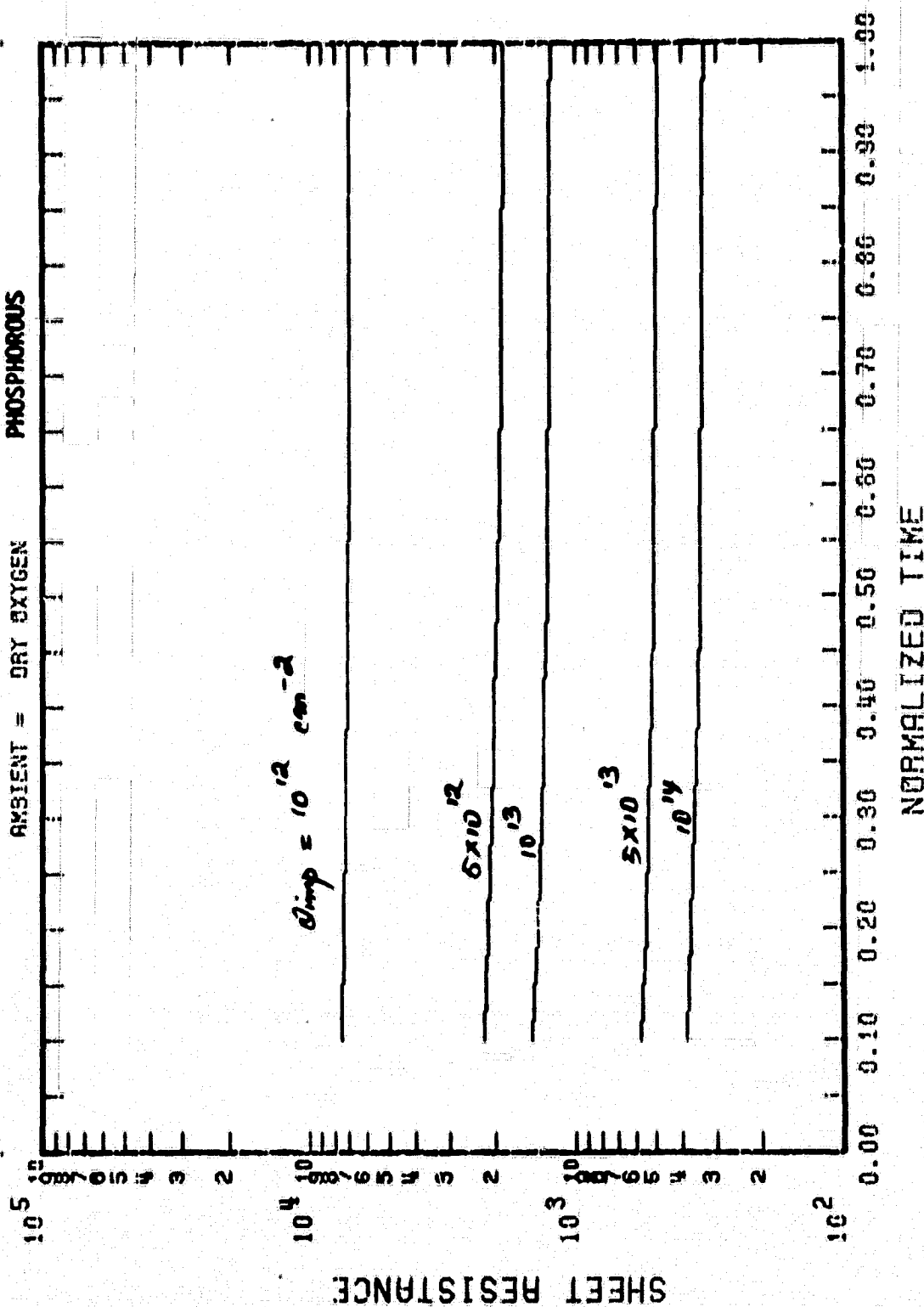


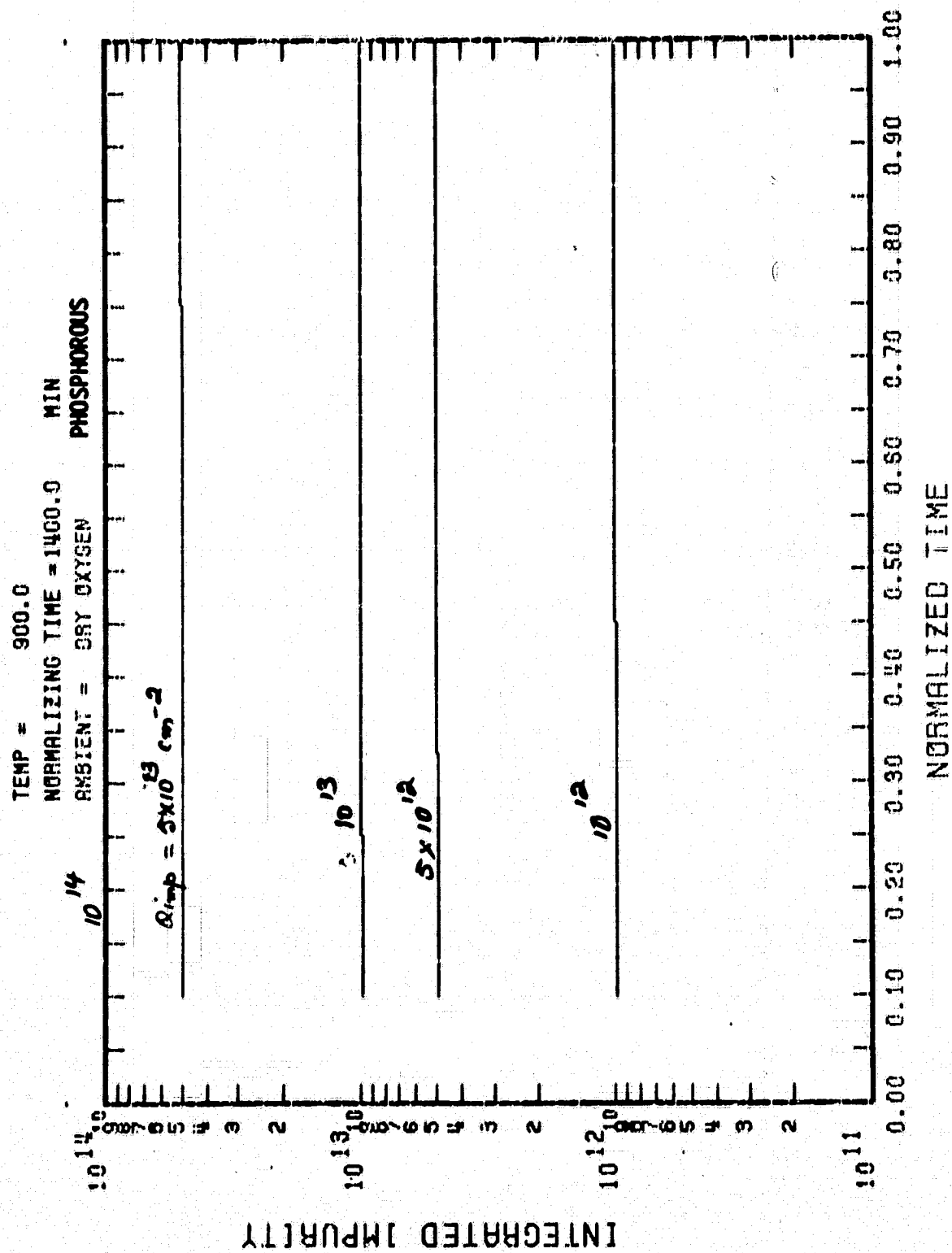
λ^2
 TEMPERATURE = 0.0000
 TIME STEP = 1000.
 TIME = 100
 TIME = 7200.00



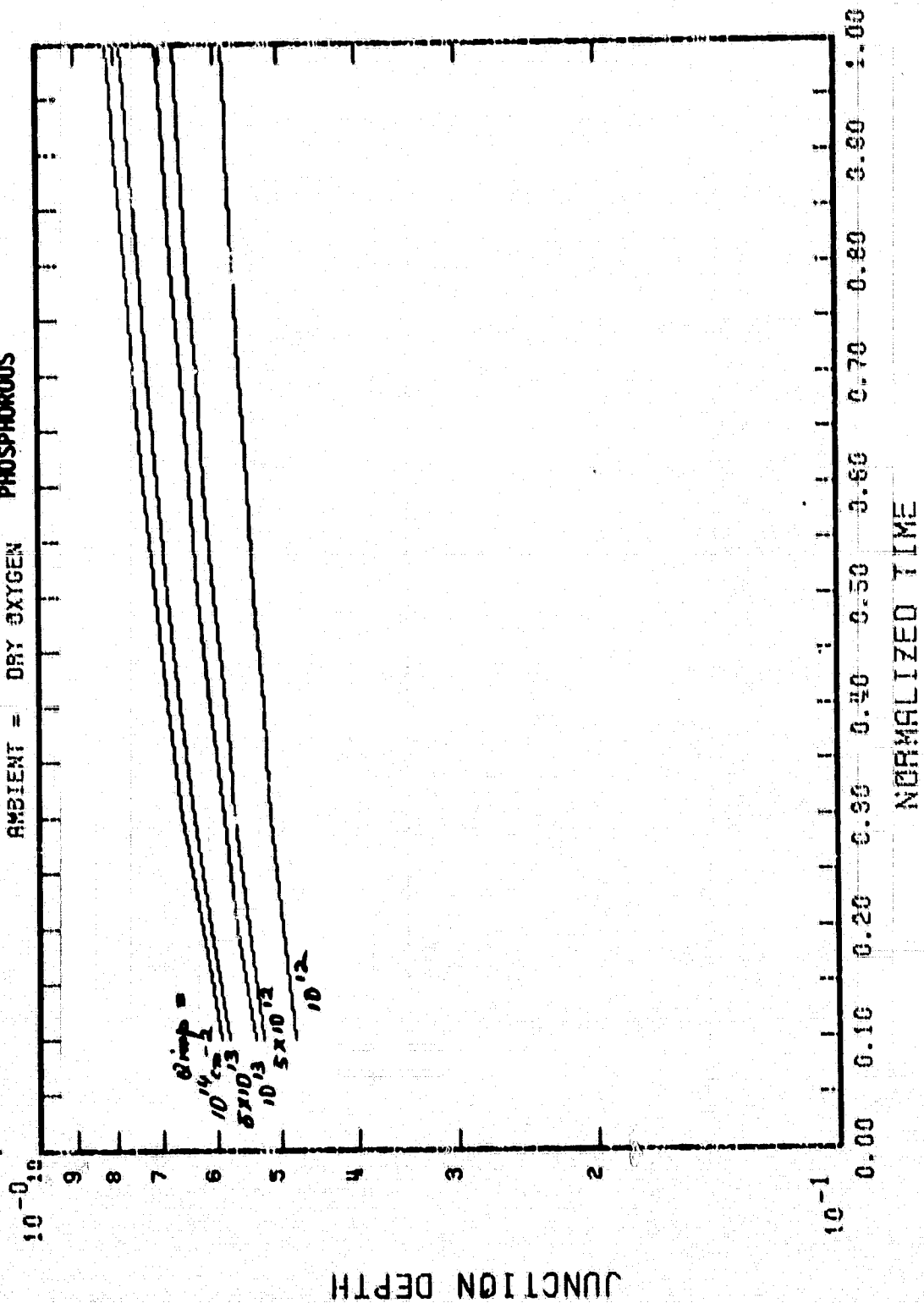


TEMP = 900.C
 NORMALIZING TIME = 1400.0 MIN
 AMBIENT = DRY OXYGEN PHOSPHOROUS

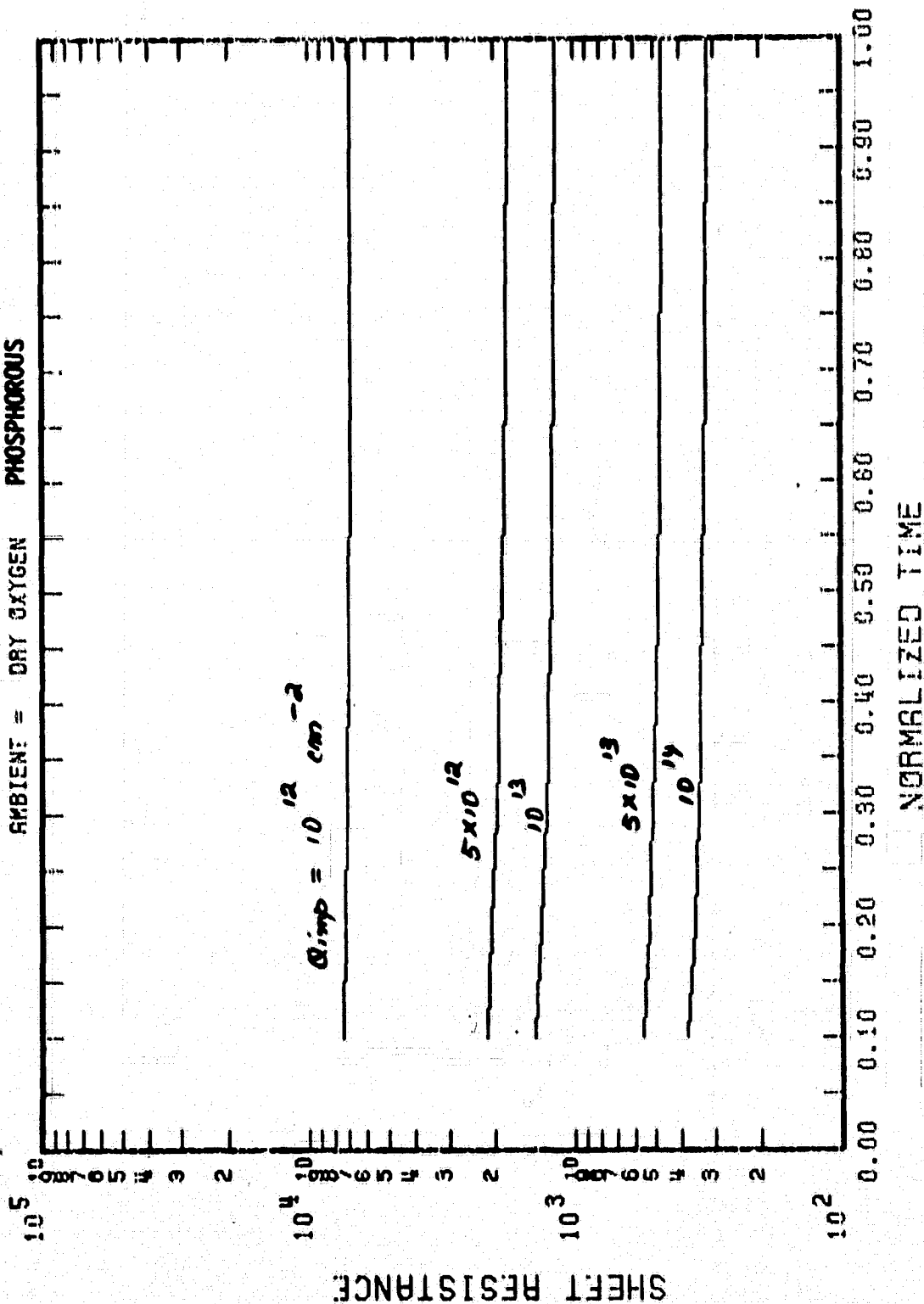




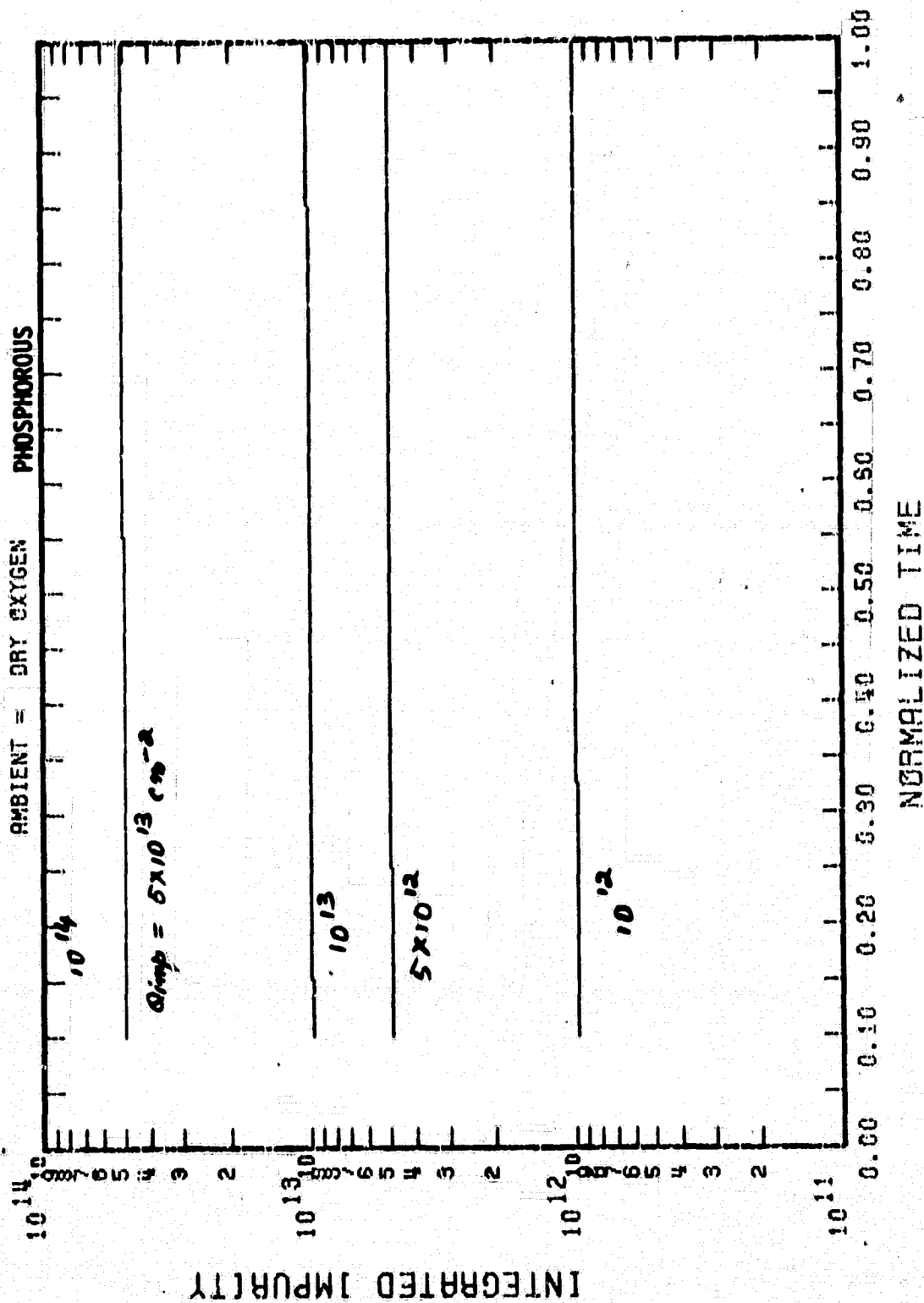
TEMP = 950.0 THICKNESS = 0.0 CM-4
 NORMALIZING TIME = 483.3 MIN
 AMBIENT = DRY OXYGEN PHOSPHOROUS



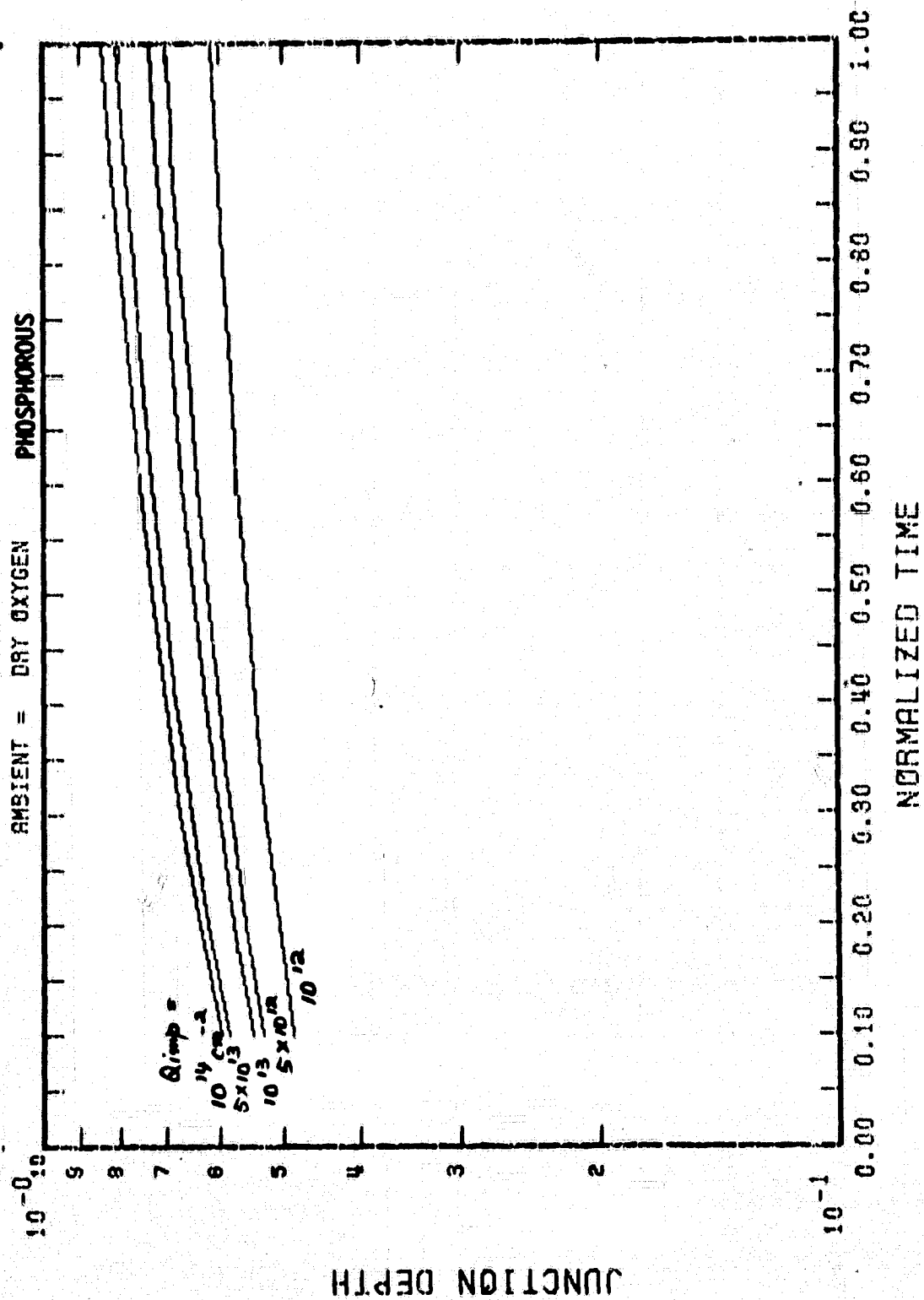
TEMP = 950.0
 NORMALIZING TIME = 483.3 MIN
 AMBIENT = DRY OXYGEN PHOSPHOROUS



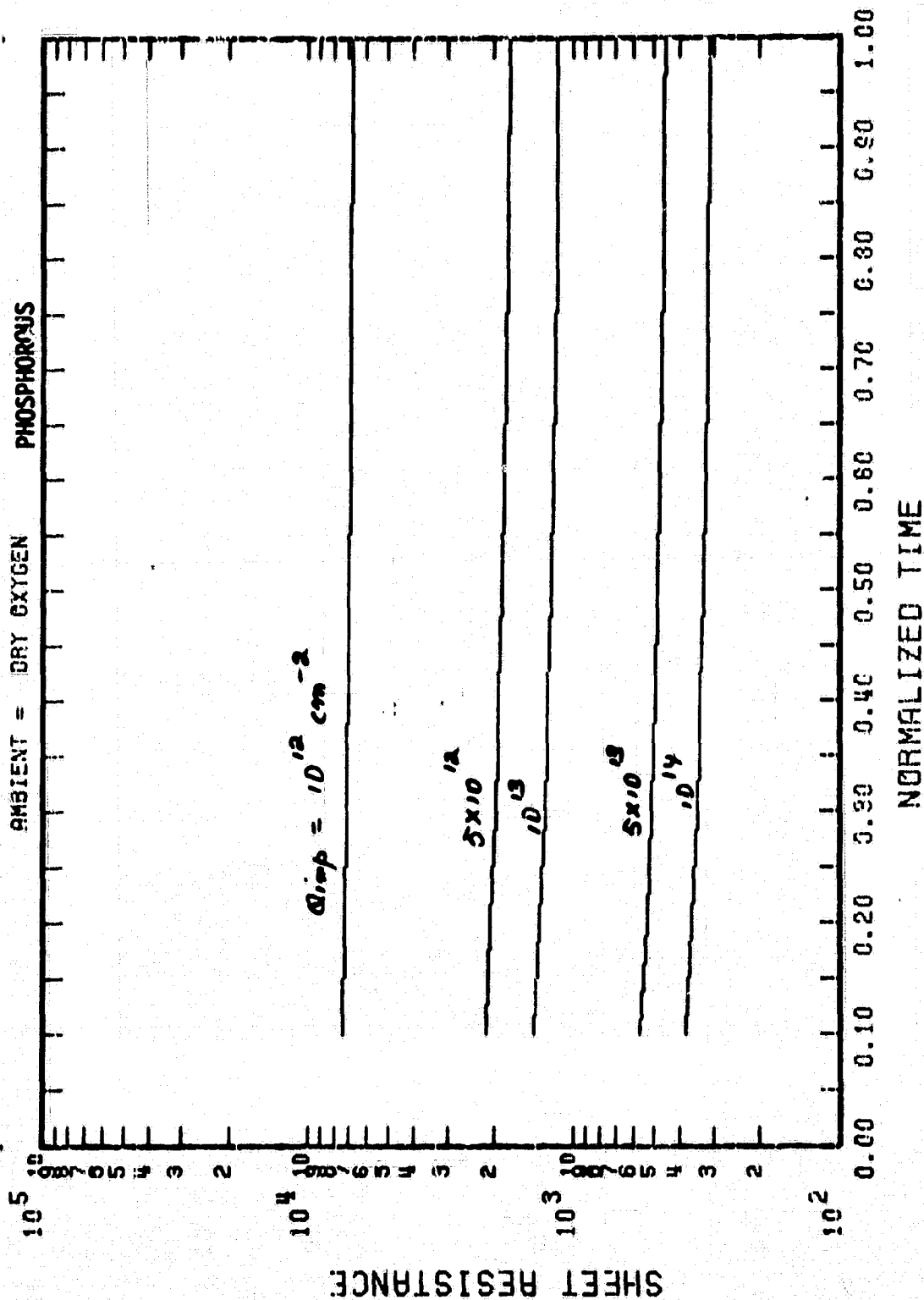
TEMP = 950.0
 NORMALIZING TIME = 483.3 MIN
 AMBIENT = DRY OXYGEN
 PHOSPHOROUS

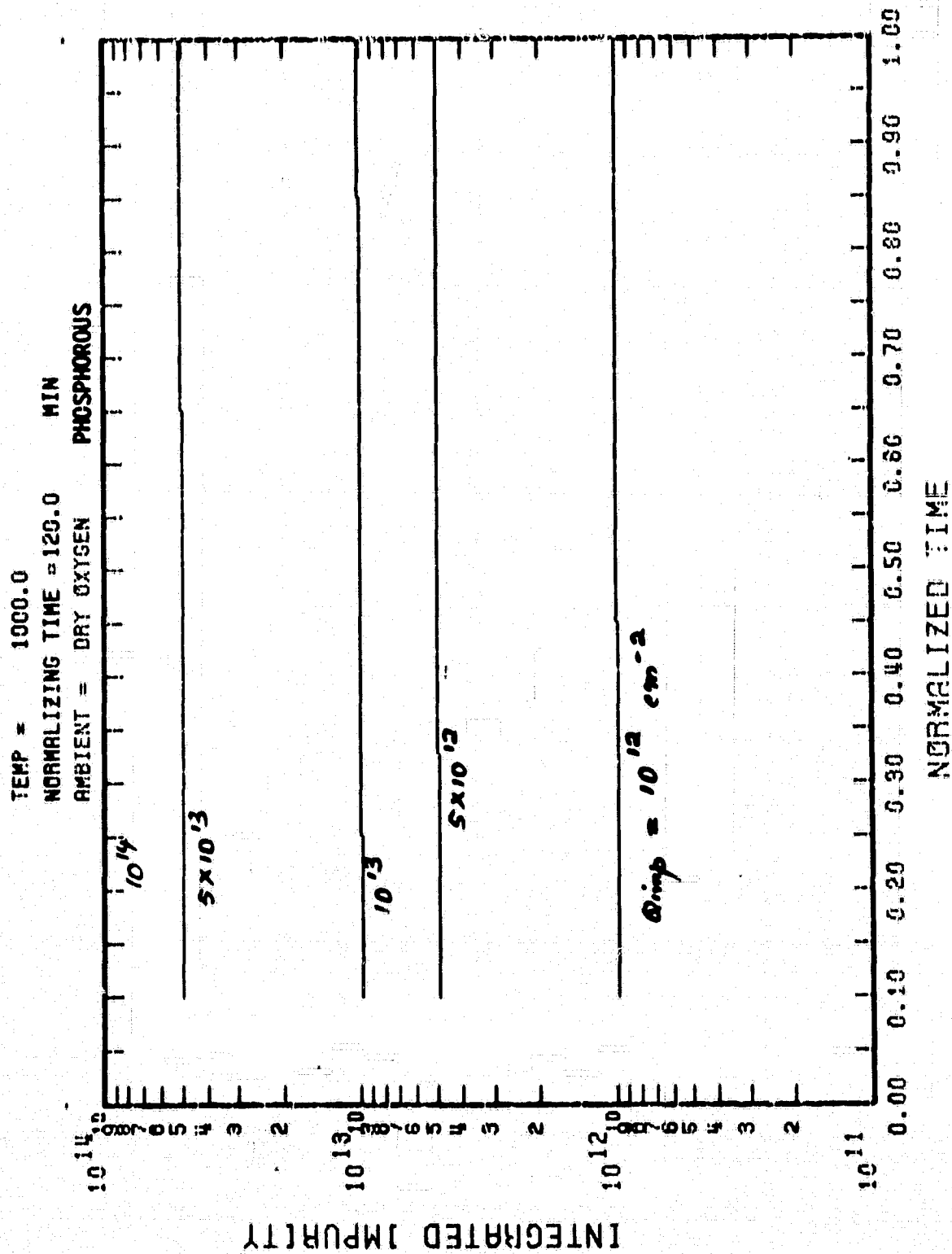


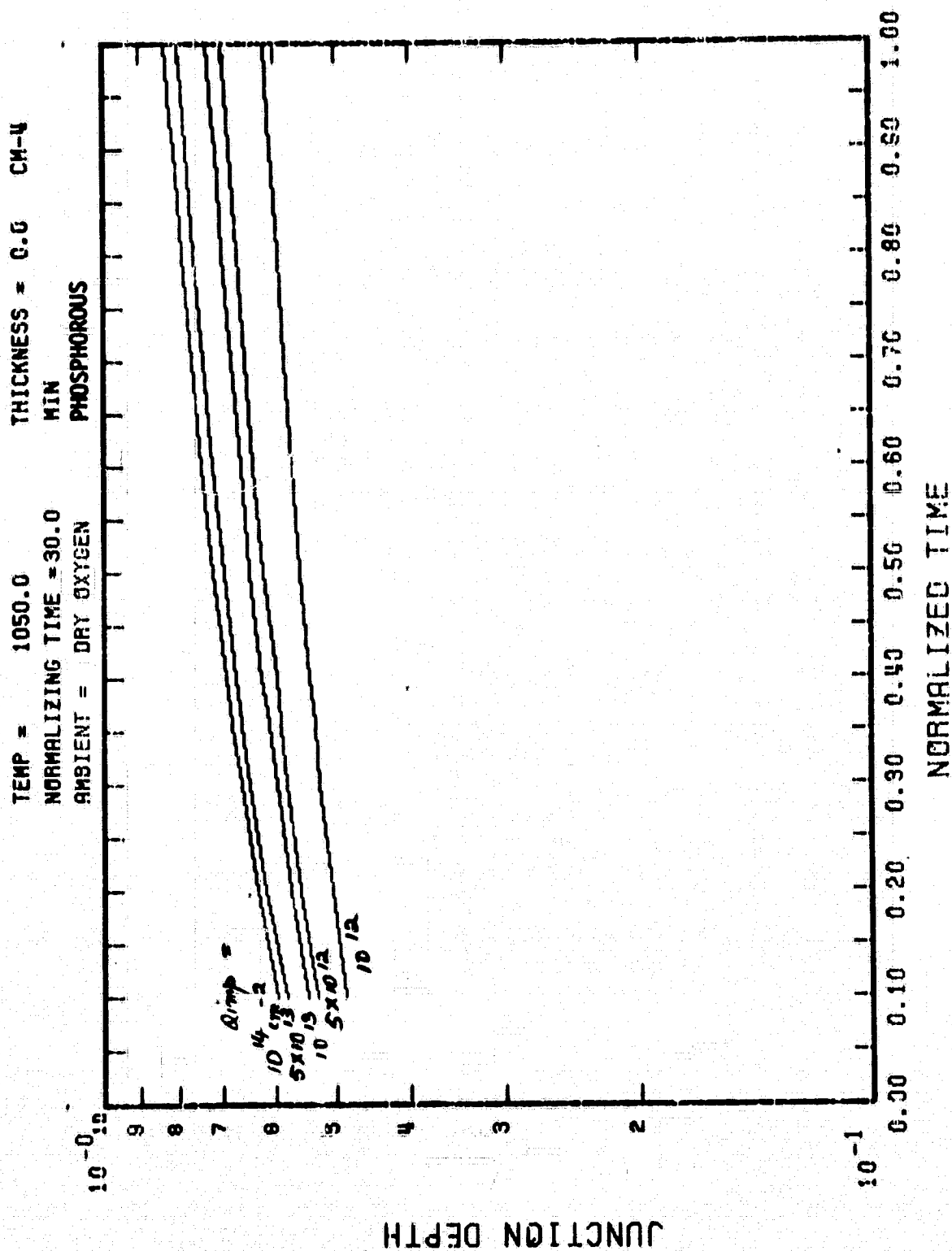
TEMP = 1000.0 THICKNESS = 0.0 CM-4
 NORMALIZING TIME = 120.0 MIN
 AMBIENT = DRY OXYGEN PHOSPHOROUS



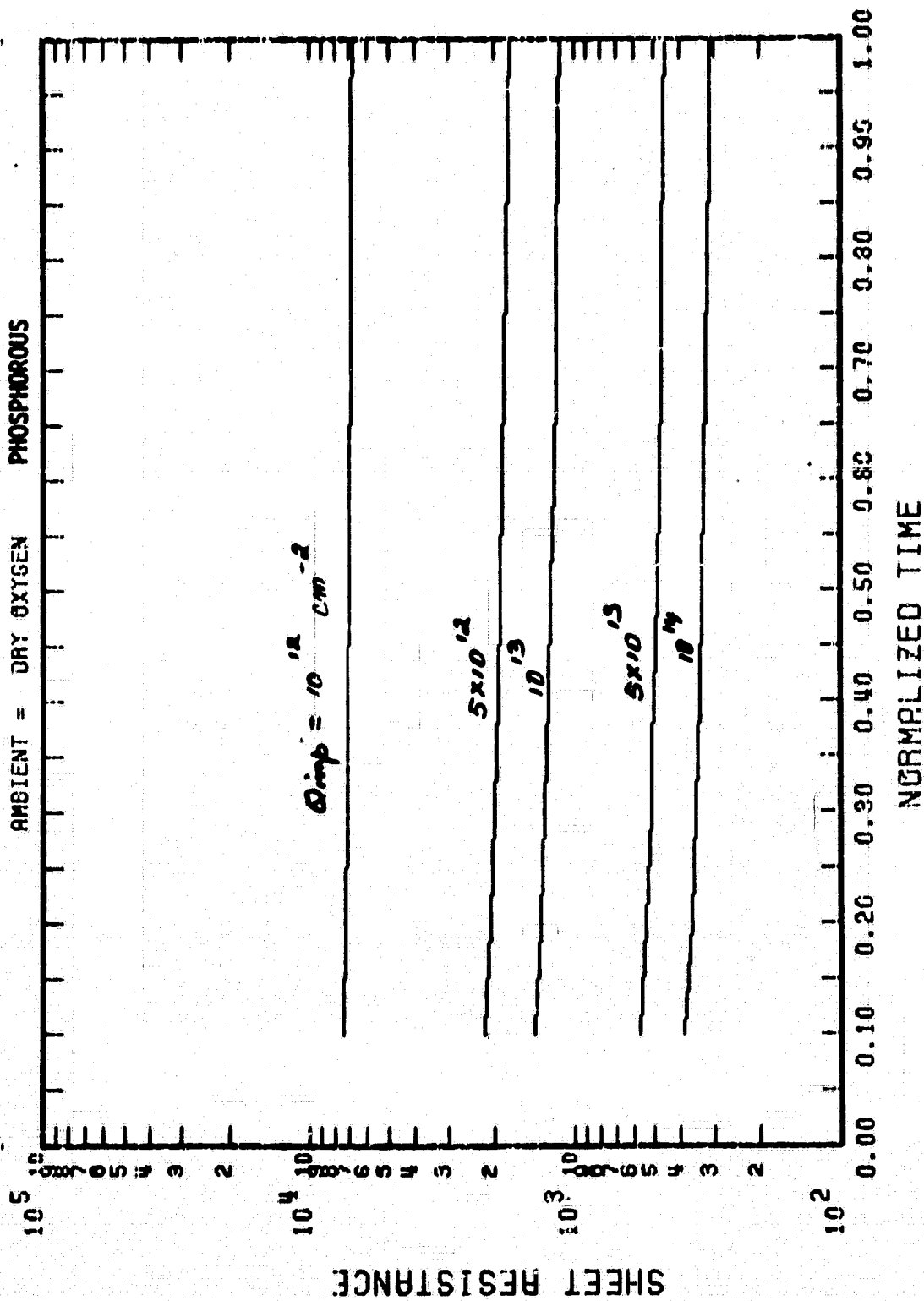
TEMP = 1000.0
 NORMALIZING TIME = 120.0 MIN
 AMBIENT = DRY OXYGEN PHOSPHOROUS

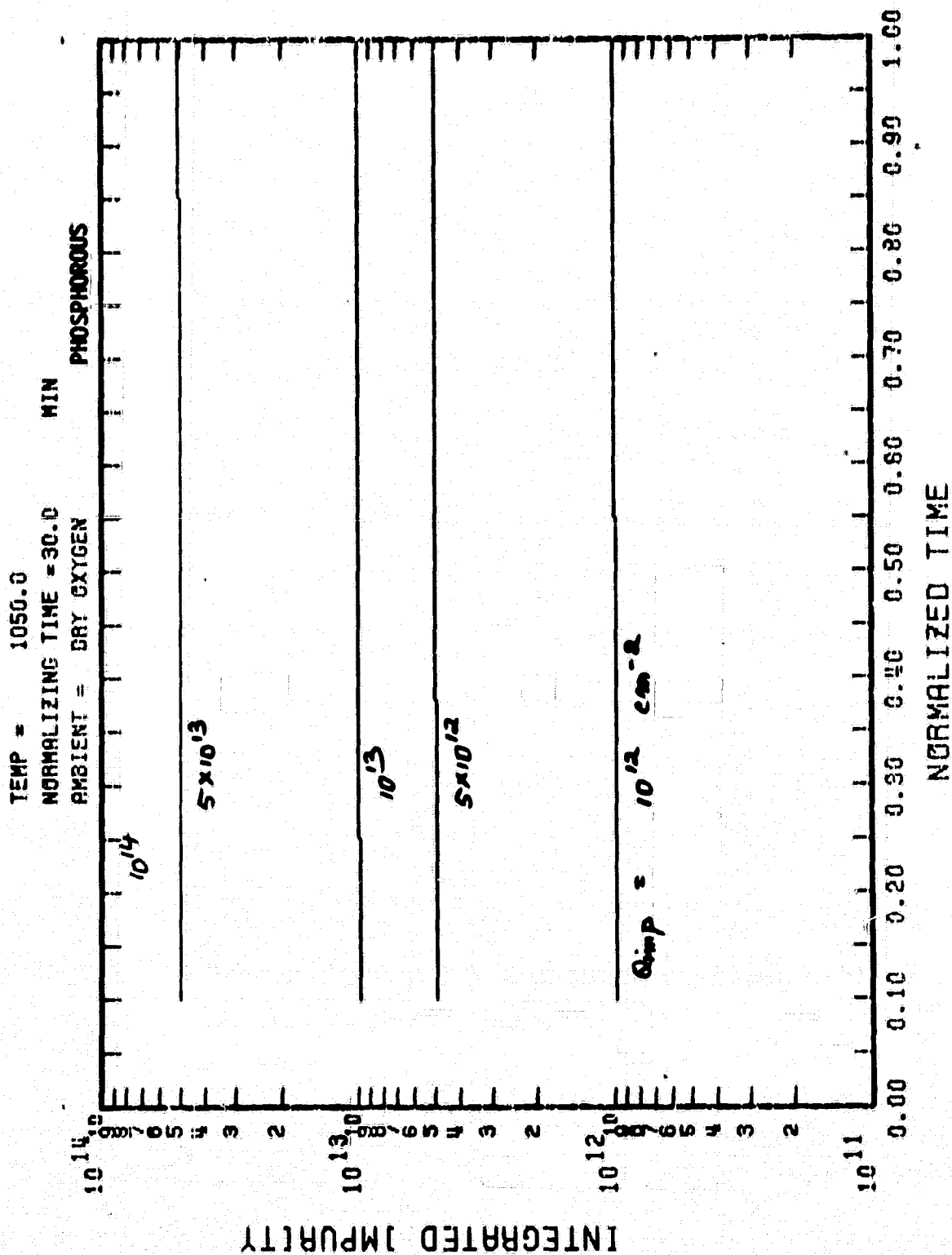




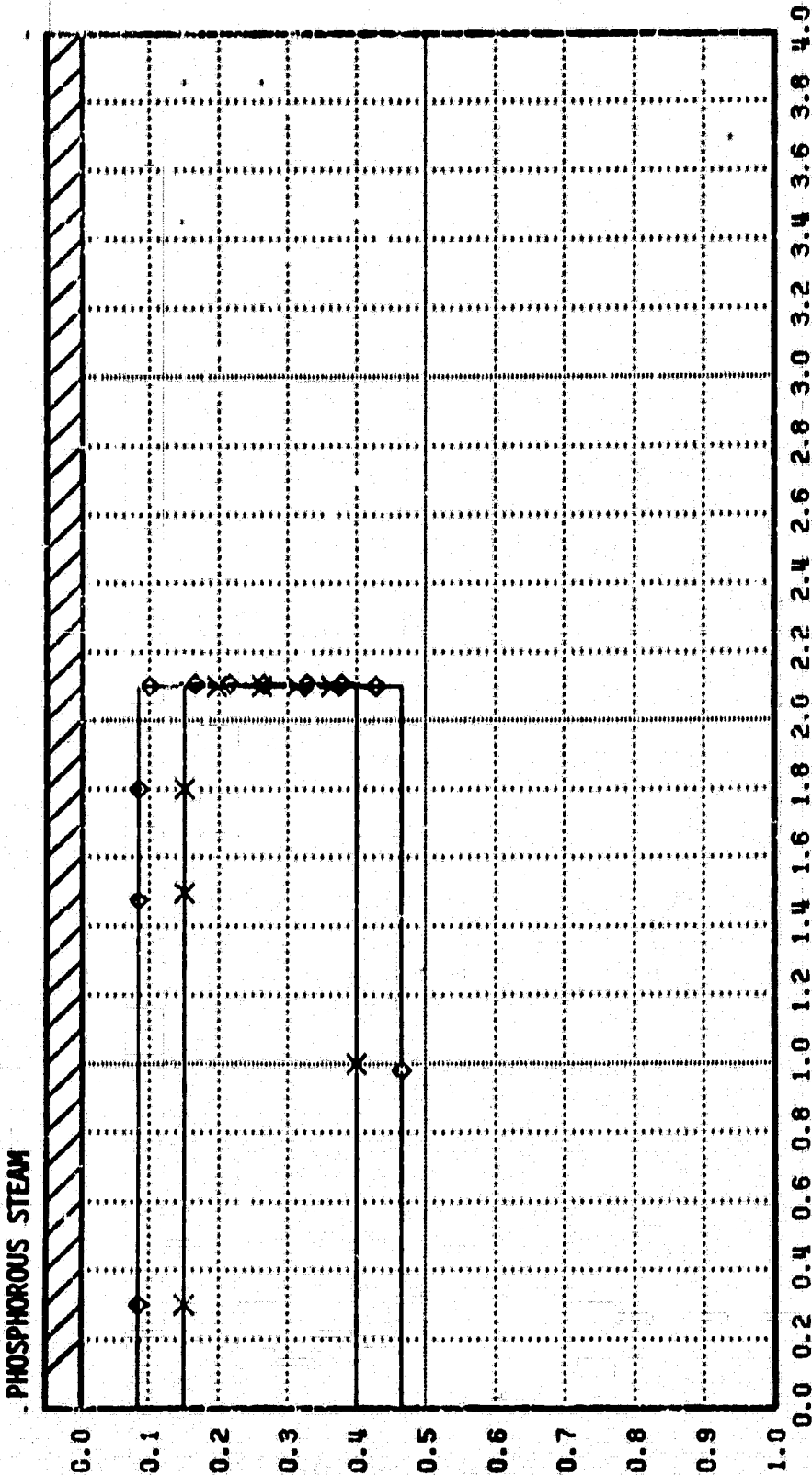


TEMP = 1050.0
 NORMALIZING TIME = 30.0 MIN
 AMBIENT = DRY OXYGEN PHOSPHOROUS



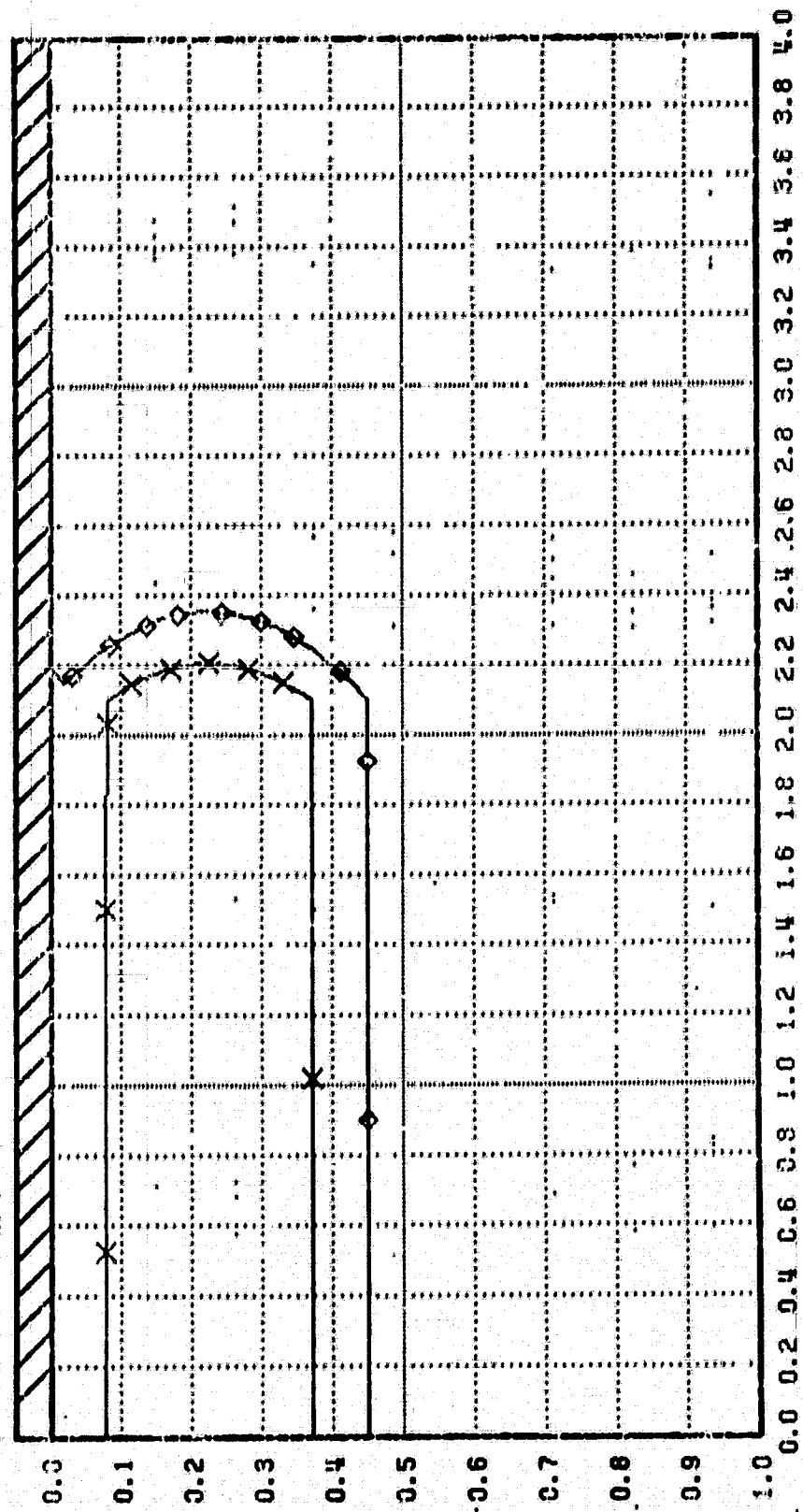


λ^2
 TEMPERATURE = 0.0000
 TIME STEP = 1000.
 TIME = 0
 = 0.00
 PHOSPHOROUS STEAM



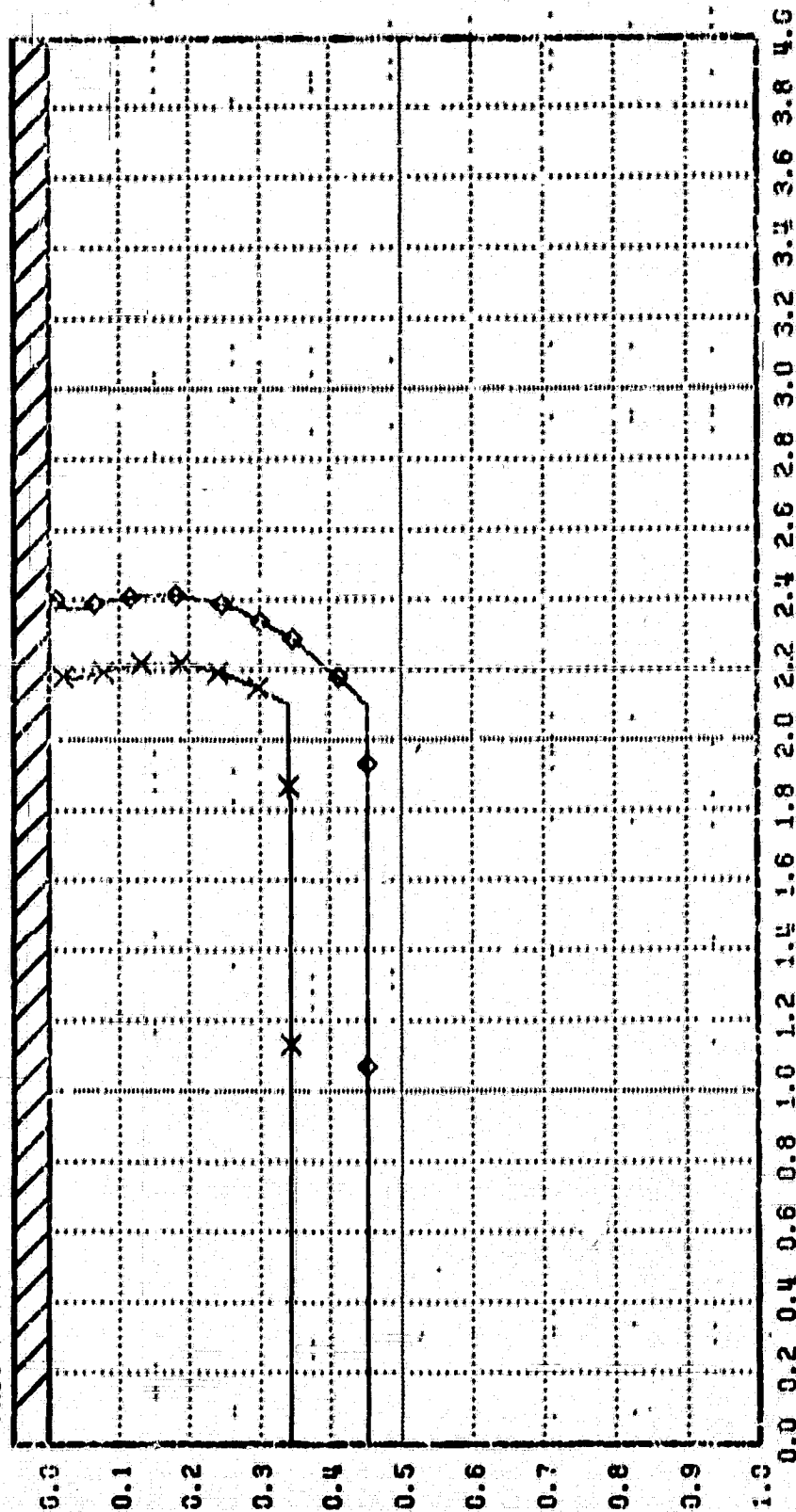
λ^2
 TEMPERATURE = 0.0000
 TIME STEP = 1000.
 TIME = 20
 PHOSPHOROUS STEAM
 = 720.00

E - 1.0E20
 O - 1.0E19
 A - 1.0E18
 + - 1.0E17
 X - 1.0E16
 D - 1.0E15



λ^2
 TEMPERATURE = 1000.
 TIME STEP = 60
 TIME = 2160.00

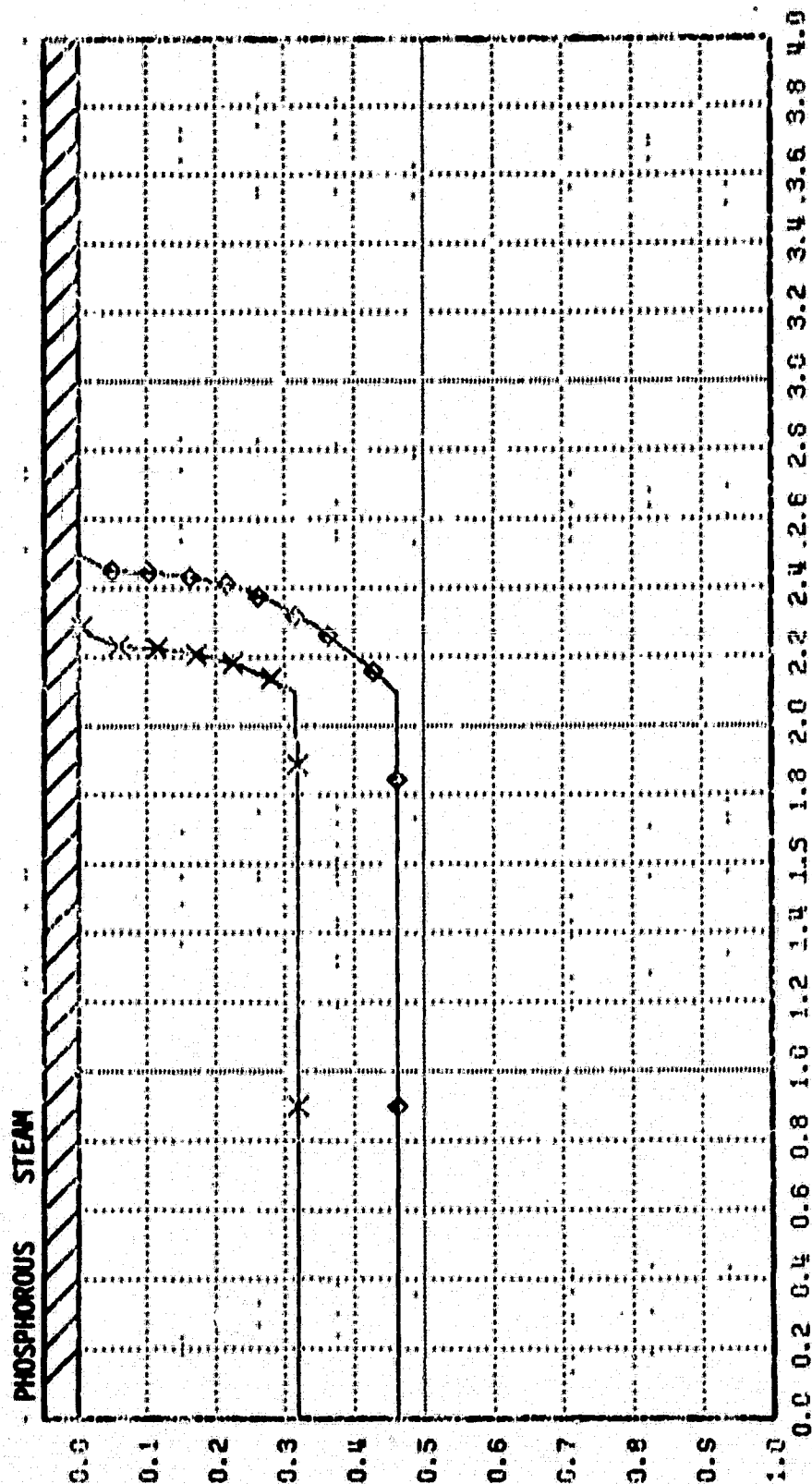
PHOSPHOROUS STEAM



λ^2
 TEMPERATURE
 TIME STEP
 TIME

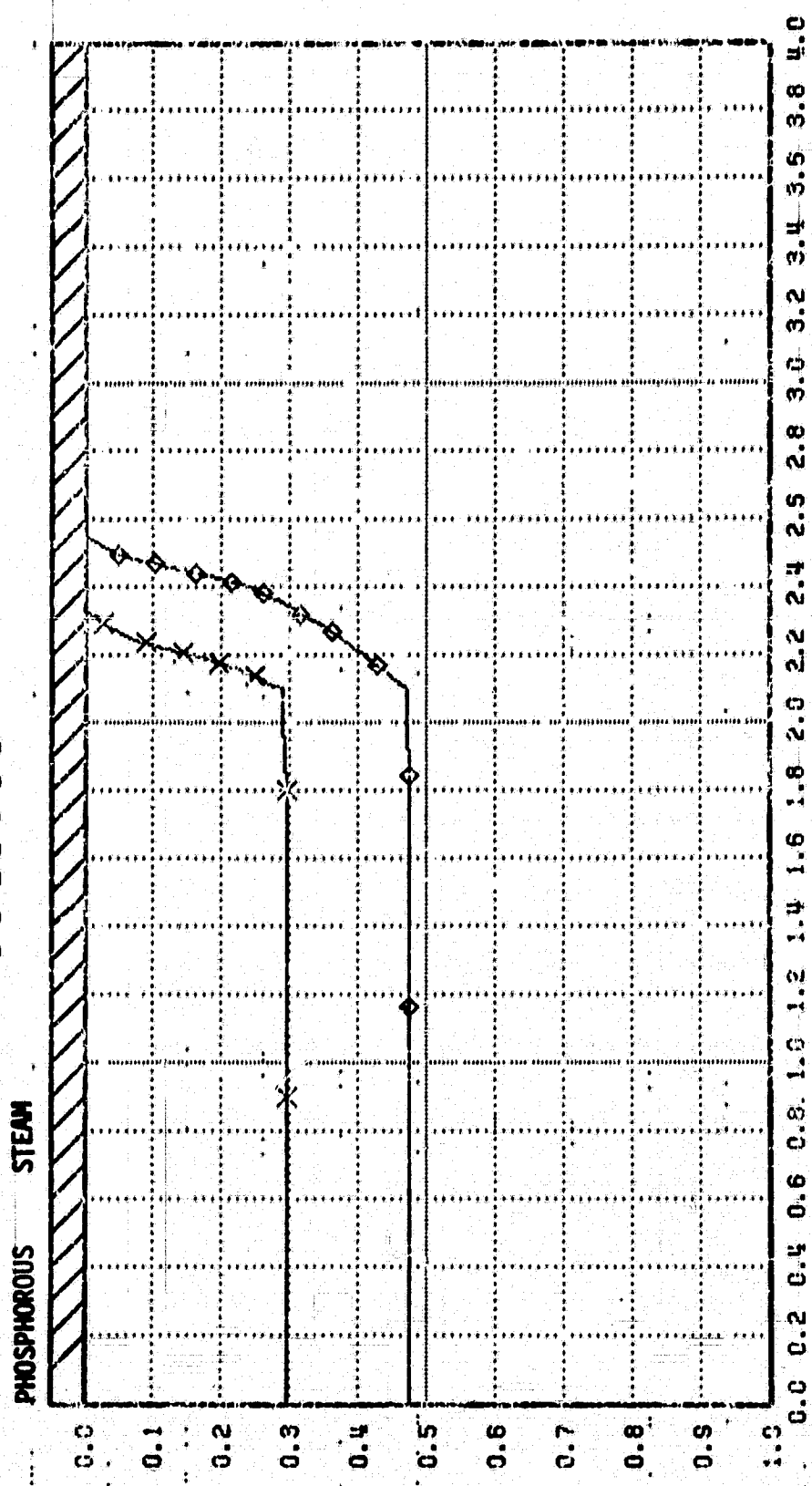
= 0.0000
 = 1000.
 = 100
 = 3600.00

- 1.0E20
 - 1.0E19
 - 1.0E18
 - 1.0E17
 - 1.0E16
 - 1.0E15

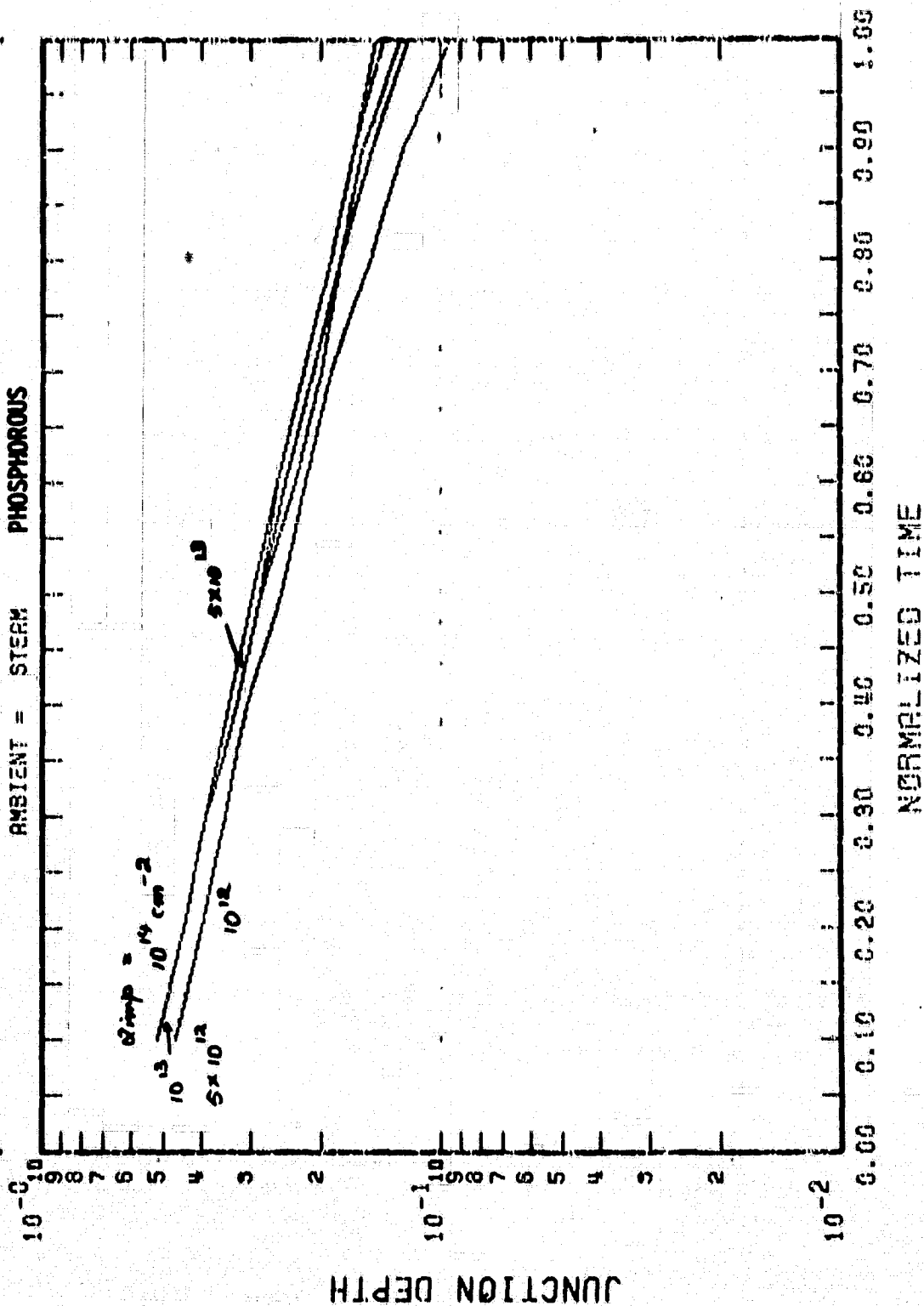


ORIGINAL PAGE IS
OF POOR QUALITY

λ^2
 TEMPERATURE = 0.0000
 TIME STEP = 1000.
 TIME = 140
 TIME = 5040.00

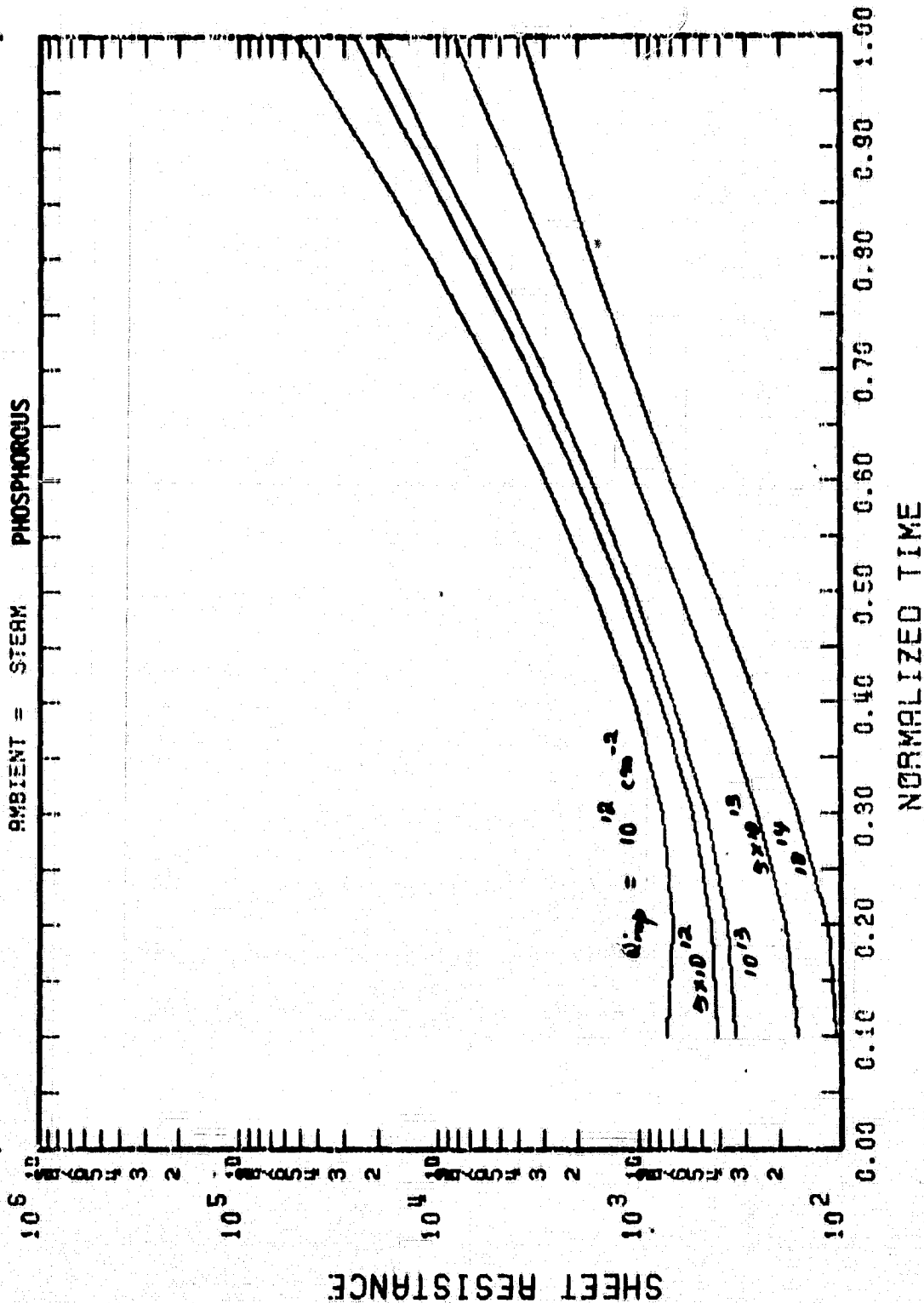


TEMP = 900.0 THICKNESS = 0.0 CM-4
 NORMALIZING TIME = 1400.0 MIN
 AMBIENT = STERN PHOSPHOROUS

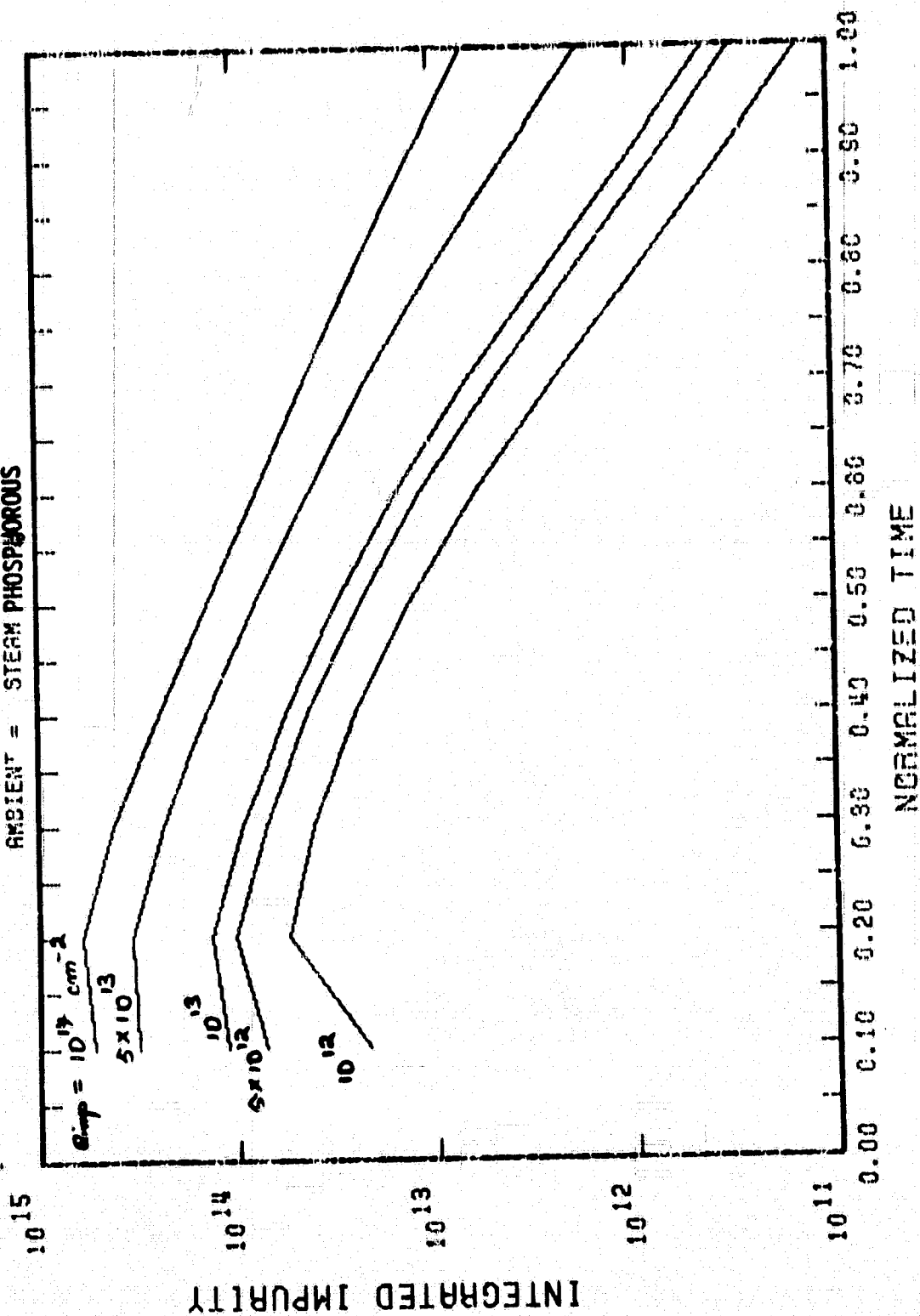


47

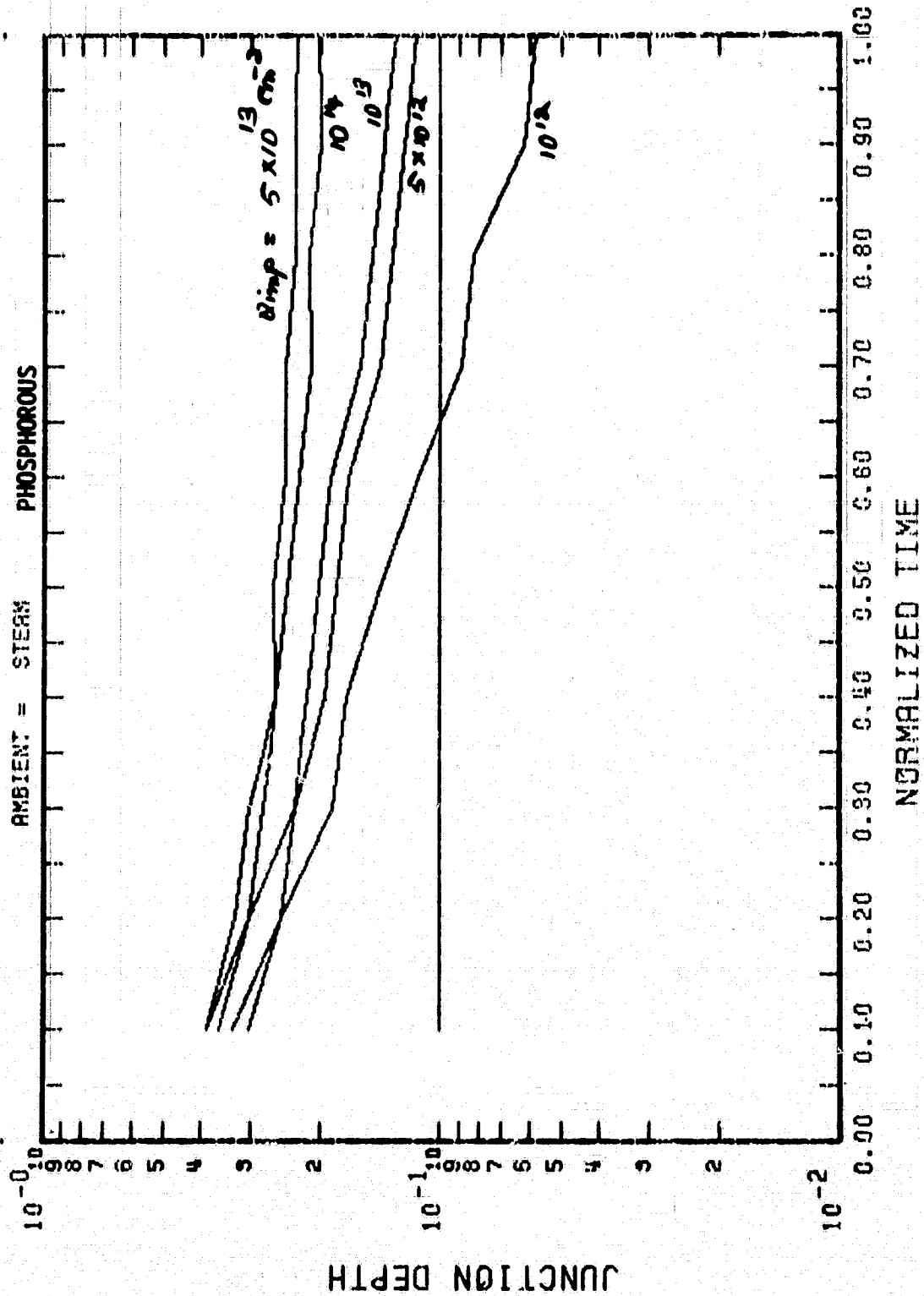
TEMP = 900.0
 NORMALIZING TIME = 1400.0 MIN
 AMBIENT = STEAM PHOSPHOROUS



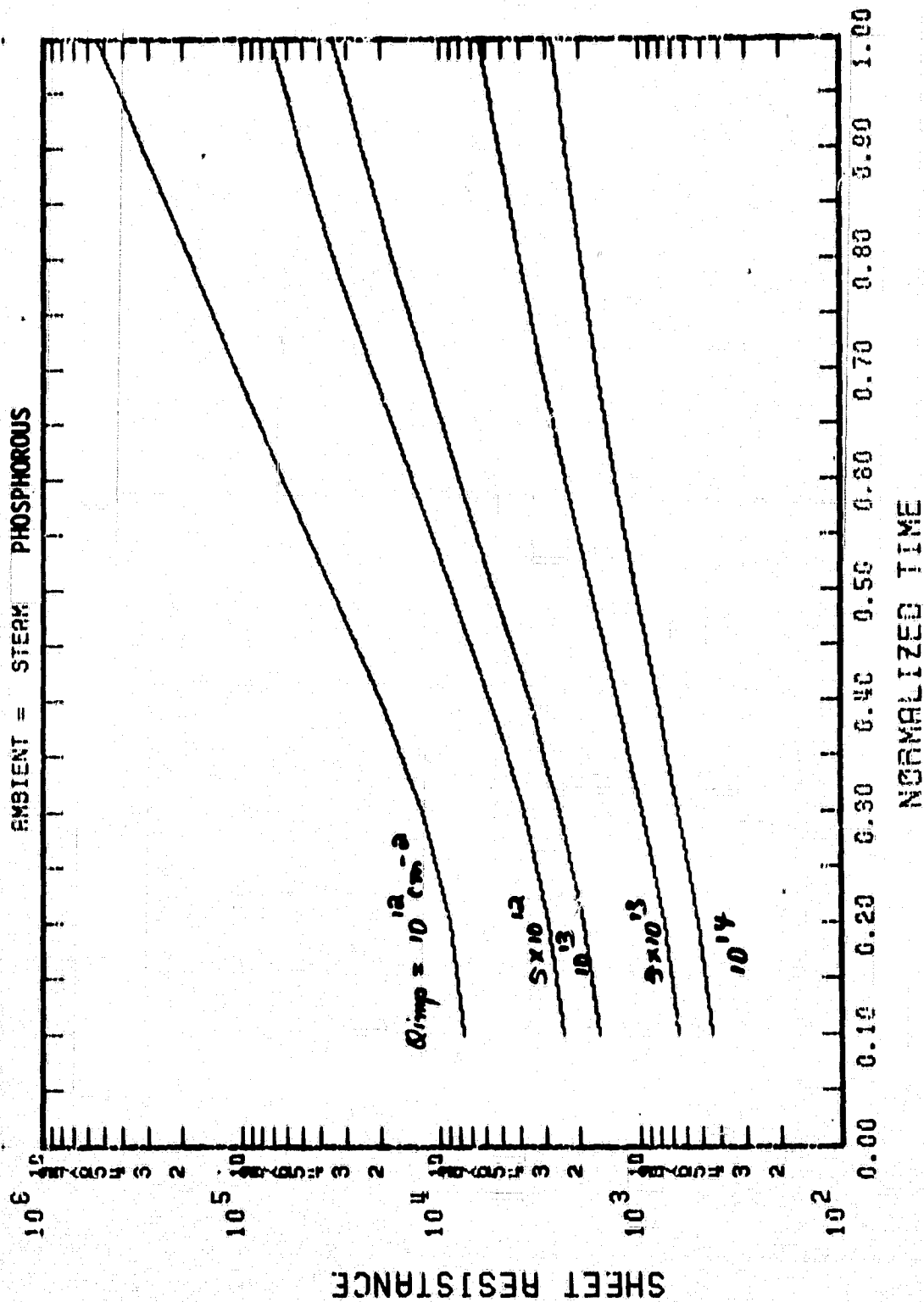
TEMP = 900.0
 NORMALIZING TIME = 1400.0 MIN
 AMBIENT = STEAM PHOSPHOROUS



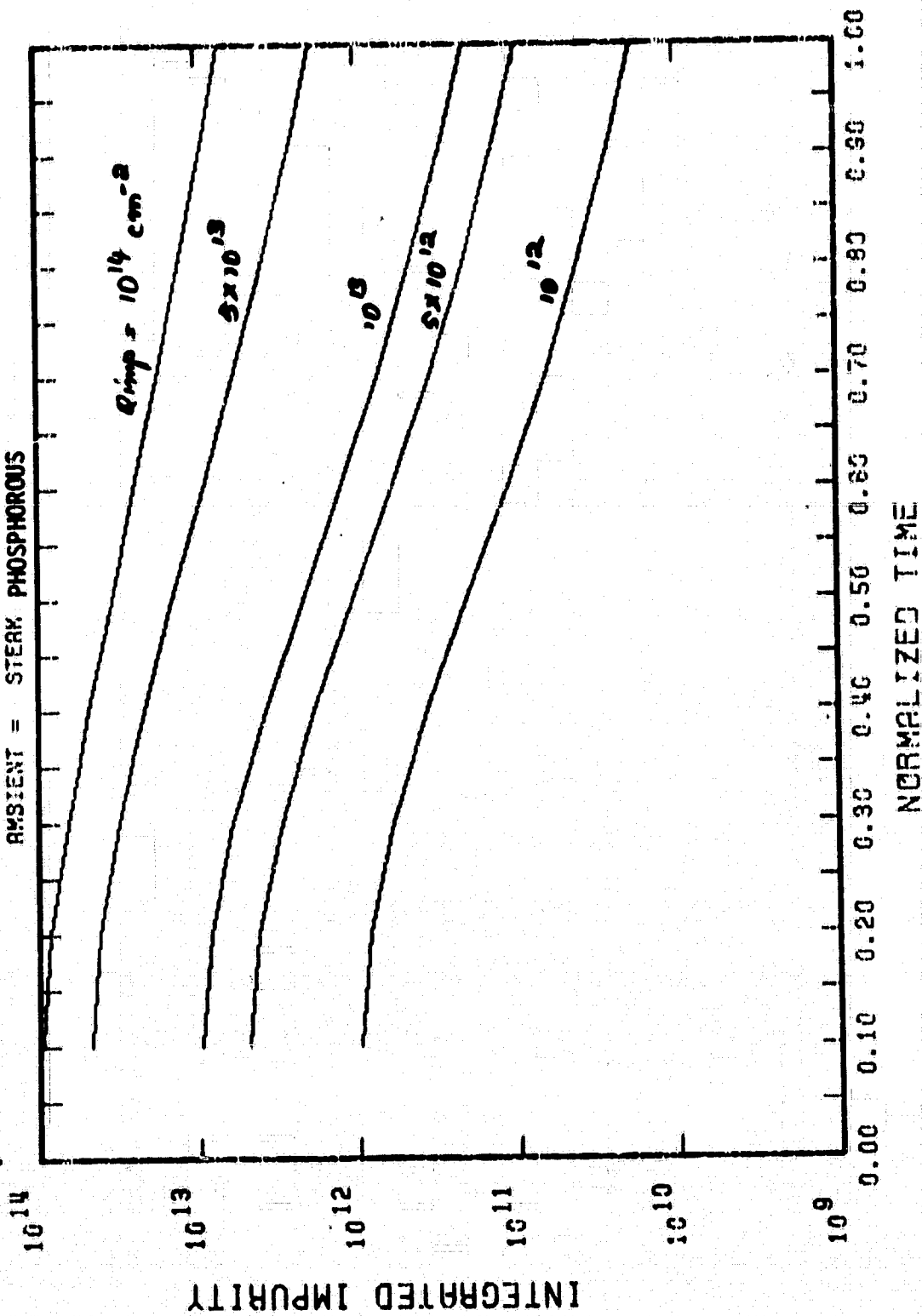
TEMP = 950.0 THICKNESS = 0.0 CM-4
 NORMALIZING TIME = 483.3 MIN
 AMBIENT = STEAM PHOSPHOROUS



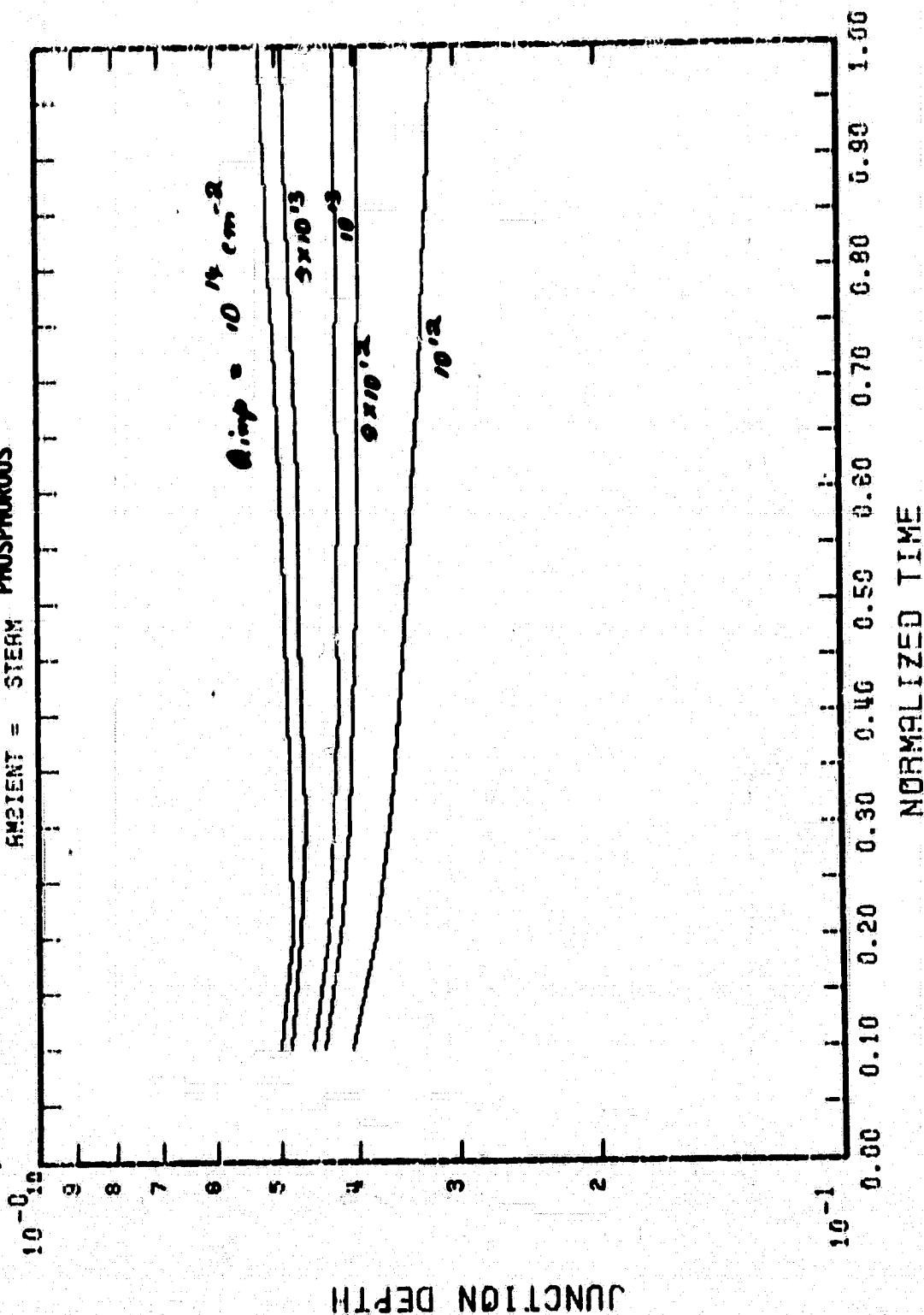
TEMP = 950.0
 NORMALIZING TIME = 483.3 MIN
 AMBIENT = STEAM PHOSPHOROUS



TEMP = 950.0
 NORMALIZING TIME = 493.3 MIN
 AMBIENT = STEAK PHOSPHOROUS



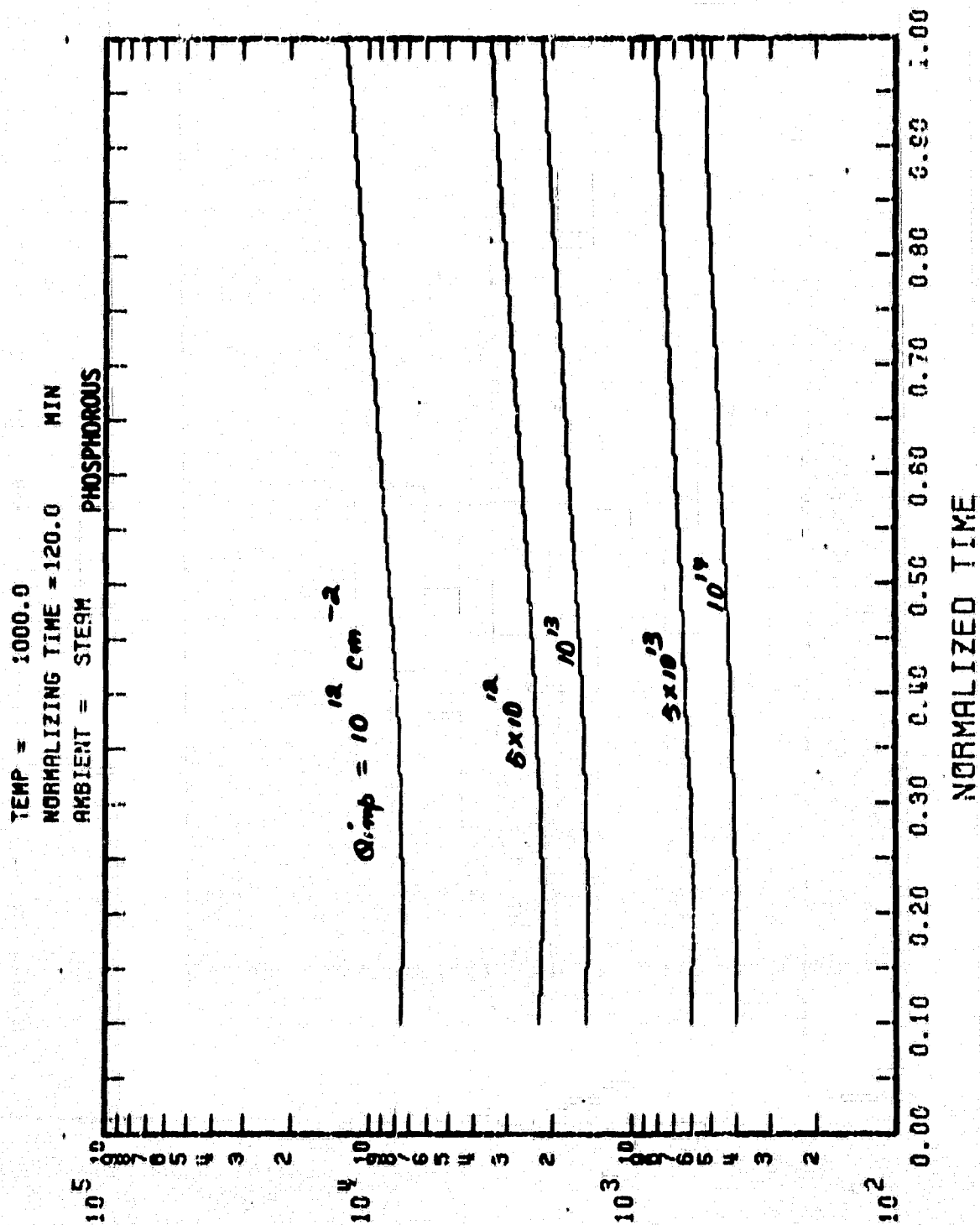
TEMP = 1000.0 THICKNESS = 0.0 CM-4
 NORMALIZING TIME = 120.0 MIN
 AMBIENT = STEAM PHOSPHOROUS



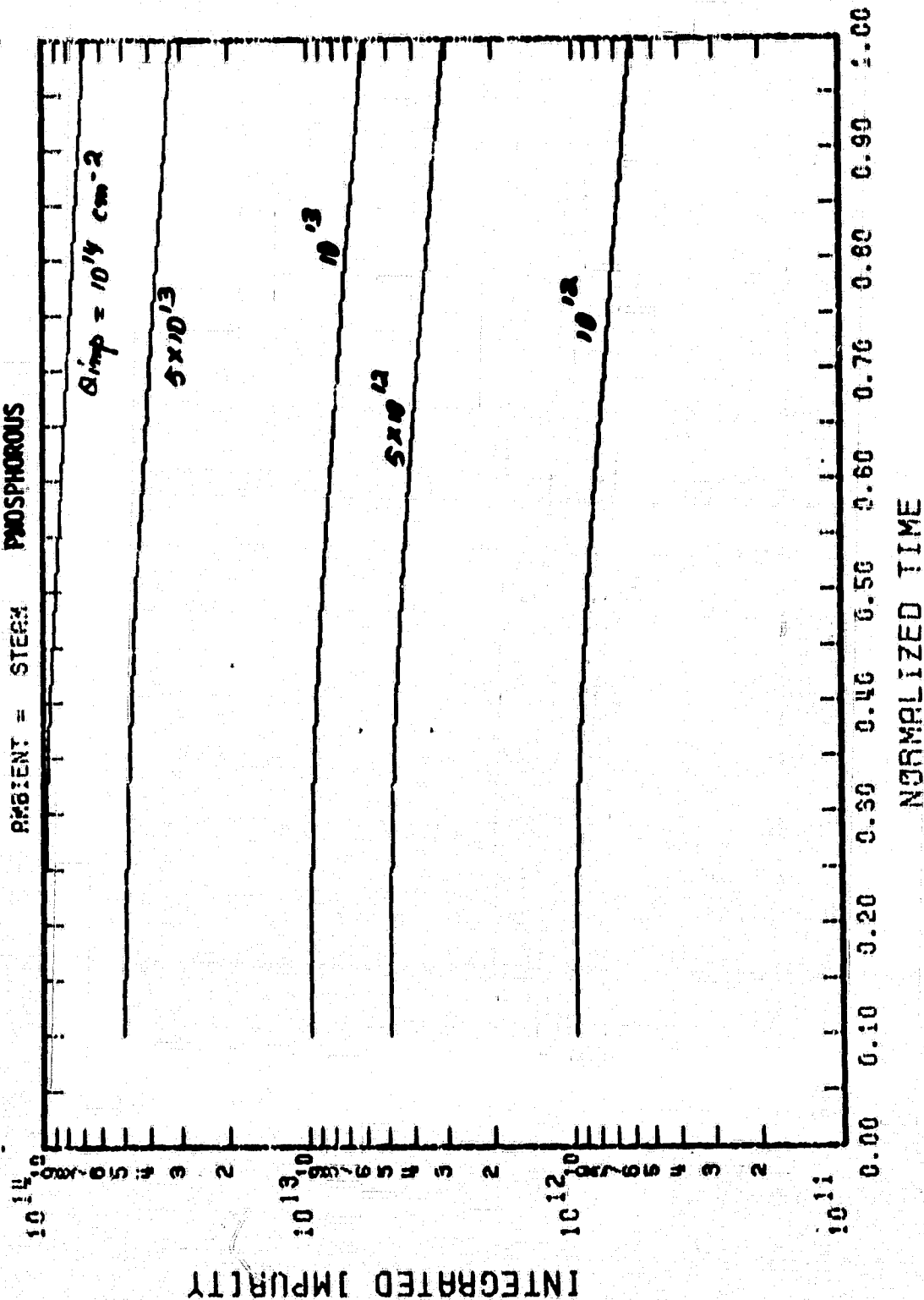
JUNCTION DEPTH

SHEET RESISTANCE

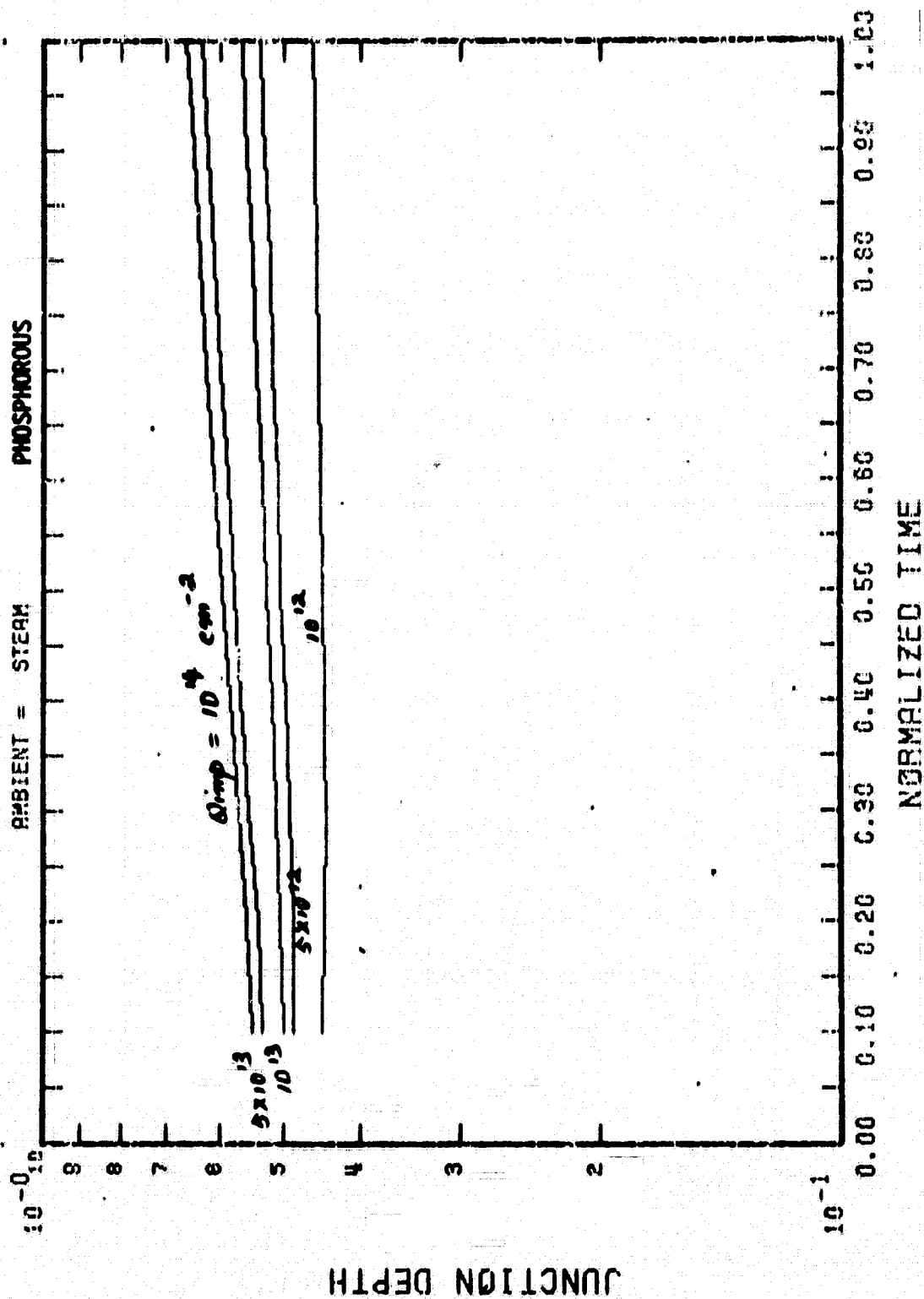
154



TEMP = 1000.0
 NORMALIZING TIME = 120.0 MIN
 AMBIENT = STEEL PHOSPHOROUS

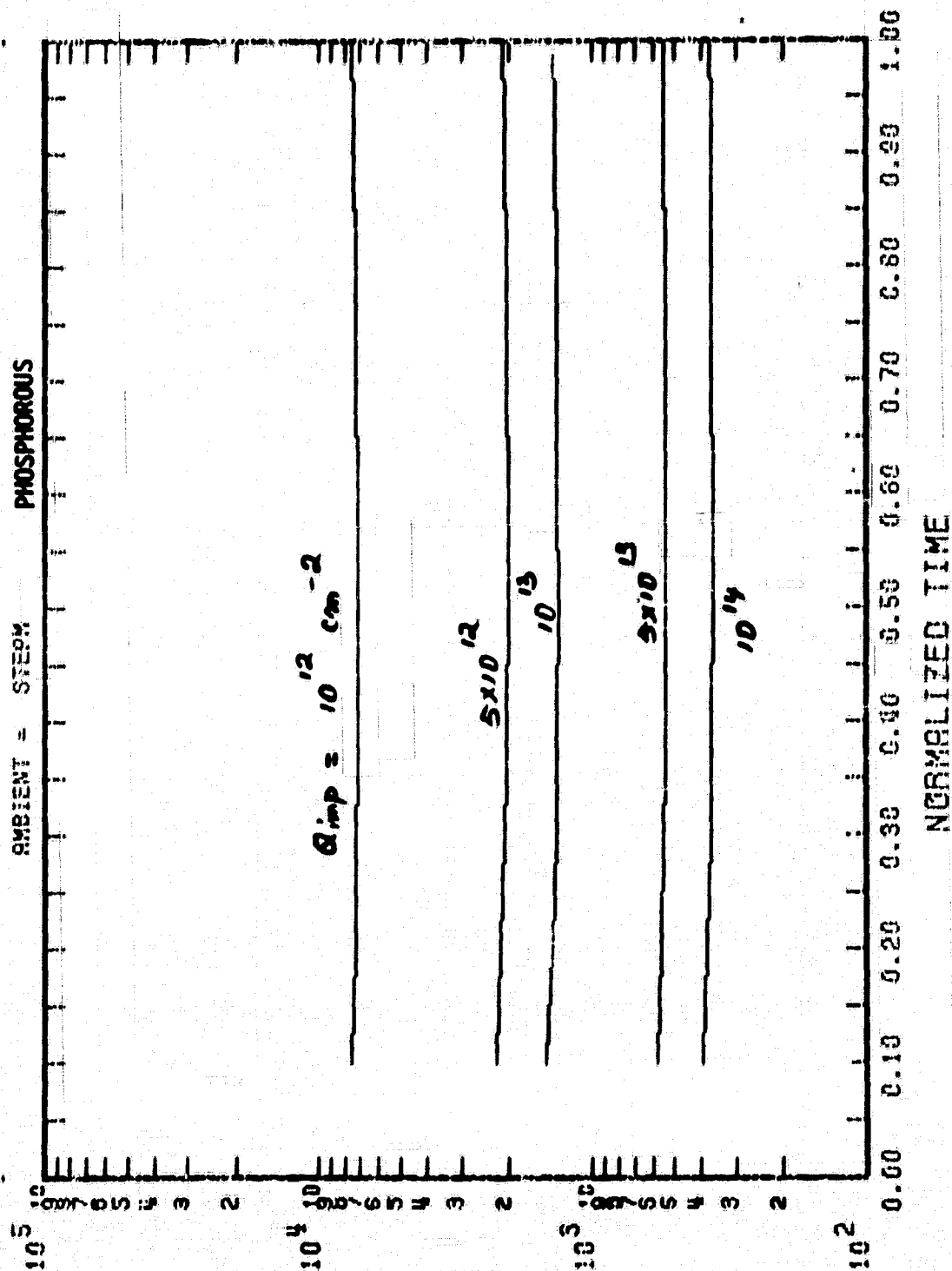


TEMP = 1050.0 THICKNESS = 0.0 CM-4
 NORMALIZING TIME = 30.0 MIN
 AMBIENT = STEAM PHOSPHOROUS

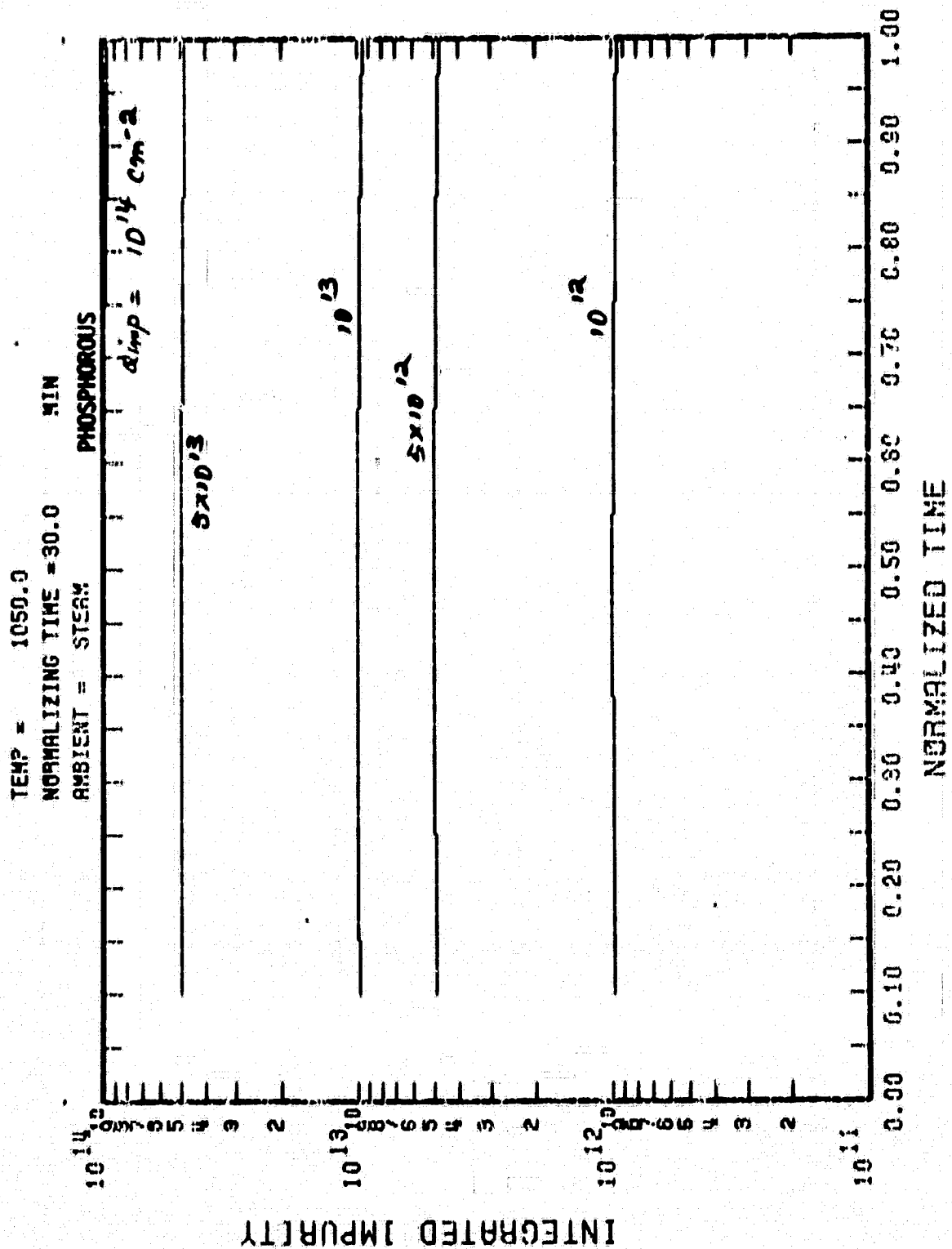


JUNCTION DEPTH

TEMP = 1050.0
 NORMALIZING TIME = 30.0 MIN
 AMBIENT = STEP PHOSPHOROUS



SHEET RESISTANCE



APPENDIX C

REVISED PROGRAM LISTING

4ICRON=5452(1).SHMLOT

```

1  C *** SHMLOT IN PLOT PROGRAM ***
2
3  C *** DATA DECK ***
4
5  C *** 1ST CARD
6  NPLT = N OF DATA SET (FOR DIFF. VALUES OF IMPLNT. DOSES)
7  NSTP1 TO NSTP5 = N OF TIME STEPS FOR A VALUE OF NPLT (MAX. 5 VALUES)
8  FIELD #110
9
10 C *** 2ND CARD, 4TH AND 6TH CARD
11 IX, IY = X AND Y AXIS LABELS RESPECTIVELY
12 1ST, 2ND AND 3RD PLOTS ARE RS, X, AND Q VS TIME PLOTS RESP.
13 JCOD = PUT N FOR NO GRID
14 FIELD 2(15A6), 2(110)
15
16 C *** 3RD CARD
17 JGRID = N OF DIV. IN Y AXIS
18 IGRID = N OF DIV. IN X AXIS
19 NYSTP = SUBGRID DIV. IN Y AXIS
20 1 GIVES 10 SUBGD.
21 NXSTP = SUBGRID DIV. IN X AXIS
22 2 GIVES 10 SUBGD.
23 YMINV = MIN VAL IN Y AXIS
24 YMAXV = MAX VAL IN Y AXIS
25 XMINV = MIN VAL IN X AXIS
26 XMAXV = MAX VAL IN X AXIS
27 FIELD 4(10), 4(10), 5
28 DIMENSION RS(10,100), XJ(10,100), Q(10,100), TIME(10,100)
29 DIMENSION XI(10,100)
30 DIMENSION IX(5), IY(5), IL(2), XO(10,100)
31
32 C *** READ IN DATA
33 READ 100, NPLT, NSTP1, NSTP2, NSTP3, NSTP4, NSTP5
34 DO 10 I=1, NPLT
35 IF(I.EQ.1) NSTP=NSTP1
36 IF(I.EQ.2) NSTP=NSTP2
37 IF(I.EQ.3) NSTP=NSTP3
38 IF(I.EQ.4) NSTP=NSTP4
39 IF(I.EQ.5) NSTP=NSTP5
40 DO 10 J=1, NSTP
41 READ(14,104) JMAX, JAMBNT
42 READ(14,101) TEMP, THAX, DELY, DELY, YO, ST
43 READ(14,101) RS(1,J), XJ(1,J), Q(1,J), TIME(1,J), XO(1,J)
44 IF(JAMBNT.EQ.1) IL(1)= 'DRY OX'
45 IF(JAMBNT.EQ.1) IL(2)= 'YGEN'
46 IF(JAMBNT.EQ.2) IL(1)= 'STEAM'
47 IF(JAMBNT.EQ.2) IL(2)= 'NITROG'
48 IF(JAMBNT.EQ.3) IL(1)= 'EN'
49
50 C
51 100 FORMAT(R110)
52 101 FORMAT(1H0,6E15.9)
53 102 FORMAT(2(15A6),2(110))
54 103 FORMAT(4(10),4(10),4)
55 104 FORMAT(1H0,8(110))
56 105 FORMAT(2A6)
57 400 FORMAT(1H0,10X,'XMIN = ',5X,'XMAX = ',5X,'YMIN = ',5X,'YMAX = ',
58 //1H0,3X,4(F10.5,1X))
59
60 C
61 DATA HGT,XMAX,YMAX/0.875,7.5,5/
62 THAX=THAX/67.
63 IC=10
64
65 C *** INITIATE THE PLOT
66 DO 11 N=1,3
67 READ 102, (IX(I),I=1,4),(IY(I),I=1,5),JCOD
68 READ 103, IGRID,JGRID,NYSTP,NXSTP,YMINV,YMAXV,XMINV,XMAXV
69 PRINT 400,XMINV,XMAXV,YMINV,YMAXV
70 IF(JCOD.NE.0) ICOD=2
71 IF(JCOD.EQ.0) ICOD=3
72 CALL PLOTS(10,0,10,3)
73 CALL PLOT(1.5,1,0,-3)
74
75 C *** DRAW HORD'R
76 CALL PLOT(0.0,YMAX,2,-1)
77 CALL PLOT(XMAX,YMAX,2,-1)
78 CALL PLOT(XMAX,0,2,-1)
79 CALL PLOT(0.0,0,2,-1)
80
81 C *** DRAW GRID
82 YDIV=YMAX/LOAT(JGRID)
83 JK=1
84 DO 12 I=1,JGRID
85 DO 13 J=1,IC,NYSTP
86 VSPC=ALOG10(LOAT(J*JK))*YDIV

```

ORIGINAL PAGE IS
OF POOR QUALITY


```

80 CALL PLOT(0.0,YSPC,3)
81 CALL PLOT(0.12,YSPC,2.0)
82 CALL PLOT(XMAX-0.12,YSPC,1.00)
83 CALL PLOT(XMAX,YSPC,2.0)
84
85 JK=JK+10
86 IGRID1=IGRID-NXSTP
87 IGRID2=IGRID-1
88 XDIV=XMAX/FLOAT(IGRID)
89 DO 14 I=1,IGRID2
90 XSPC=FLOAT(I)*XDIV
91 CALL PLOT(XSPC,0.0,3)
92 CALL PLOT(XSPC,0.12,2.0)
93 CALL PLOT(XSPC,YMAX-0.12,1.00)
94 CALL PLOT(XSPC,YMAX,2.0)
95
96 C *** AXES NUMBERS
97 VAL=YMINV
98 JK=1
99 JGRD1=JGRID-1
100 DO 16 I=1,JGRD1
101 DO 17 J=1,IC,NYSTP
102 IF(I.EQ.JGRD1.AND,J.NE.1) GO TO 17
103 YSPC=ALOG10(FLOAT(J*JK))*YDIV
104 YSPC=YSPC
105 IF(J.EQ.1) GO TO 200
106 VAL=FLOAT(J)
107 CALL NUMBER(0.18,YSPC,1.00,VAL,0.1)
108 GO TO 17
109 200 VAL2=ALOG10(VAL)
110 CALL NUMBER(0.54,YSPC,1.00,10.0,0.1)
111 CALL NUMBER(0.35,YSPC,1.00,0.1,VAL2,0.1)
112
113 17 CONTINUE
114 VAL=VAL*10.
115 16 JK=JK+10
116 XV=XMAXV/FLOAT(IGRID)
117 IGRID3=IGRID+1
118 DO 18 I=1,IGRID3
119 XSPC(I)=I*XDIV*NYSTP
120 XSPC=XSPC-0.2
121 VAL=XV*(I-1)
122 C *** PUT LABELS
123 CALL SYMBOL(0.8,1.0,0.1313,1Y,90.30)
124 CALL SYMBOL(2.00,0.50,0.1313,1X,0.30)
125 CALL SYMBOL(2.0,4.5,HGT,TEMP=1.0,7)
126 CALL NUMBER(3.0,4.5,HGT,TEMP,0.1)
127 CALL SYMBOL(2.0,5.3,HGT,NORMALIZING TIME =
128 0.0,32)
129 CALL NUMBER(3.4,5.3,HGT,THAX,0.1)
130 CALL SYMBOL(2.0,5.1,HGT,AMBIENT = 1.0,10)
131 CALL SYMBOL(3.0,5.1,HGT,IL,0.12)
132 IF(IN.EQ.2) CALL SYMBOL(4.5,5.5,HGT,THICKNESS =
133 0.0,23)
134 IF(IN.EQ.2) CALL NUMBER(5.4,5.5,HGT,YDIST,0.1)
135
136 C *** DRAW CURVES
137 YLOG=YMAX/FLOAT(JGRD)
138 XVI=XMAX/XMAXV
139 YHVR=1/YMINV
140 DO 22 I=1,NPLT
141 CALL PLOT(0.0,0.0,3)
142 IF(I.EQ.1) NSTP=NSTP1
143 IF(I.EQ.2) NSTP=NSTP2
144 IF(I.EQ.3) NSTP=NSTP3
145 IF(I.EQ.4) NSTP=NSTP4
146 IF(I.EQ.5) NSTP=NSTP5
147 DO 21 J=1,NSTP
148 IF(J.EQ.1) L=3
149 IF(J.NE.1) L=2
150 IF(IAMBNT.NE.3) TIME(I,J)=TIME(I,J)/TIME(NPLT,NSTP)
151 XMOVE=TIME(I,J)*XVI
152 IF(IN.EQ.3) GO TO 201
153 IF(IN.EQ.2) GO TO 202
154 YMOVE=YLOG*ALOG10(RS(I,J)*YHVR)
155 GO TO 21
156 201 YMOVE=YLOG*ALOG10(Q(I,J)*YHVR)
157 GO TO 21
158 202 YMOVE=YLOG*ALOG10(XJ(I,J)*YHVR)
159 21 CALL PLOT(XMOVE,YMOVE,L,0)
160 IF(IN.NE.2) GO TO 22
161 CALL PLOT(0.0,0.0,3)
162 DO 23 J=1,NSTP

```

MINI

CM=4

```

160 IF(J.EQ.1) L=3
161 IF(J.NE.1) L=2
162 XMOVE=TIME(1,J)*XV1
163 X(1,J)=X(1,J)*(YD1ST-D.45*20(1,J))/1.E-4
164 IF(X(1,J).LT.1.E-01) X(1,J)=1.E-01
165 YMOVE=YLOG*ALOG(0/X(1,J)*YHVR)
23 CALL PLOT(XMOVE,YMOVE,L,0)
22 CONTINUE
166 CALL PLOT(0.,0.,999)
167 CONTINUE
168 STOP
169 END
170
171

```

1 2 3 4 5 6 7 8 9 0 1 2 3 4 5

```

SUBROUTINE PARAM(I,Y)
C .....
C      AFTER THAI AND MORIN AND MAITA.
C .....
      IMPLICIT DOUBLE PRECISION (A-H,O-Z)
      CI=1.E16
      2  FG=1.21+7.1E-10*SQRT(I)*(Y)**(-.5)
      EG=EG/(8.42E-5*(Y))
      CIOLD=CI
      CI=3.87E16*((Y)**(.15))*EXP(-EG/2.)
      R=CIOLD/CI
      IF(R.LT.0.995.AND.R.GT.1.005) GO TO 2
      RETURN
      END
C .....

```

41CN0N=5n521114G

```

1      DOUBLE PRECISION FUNCTION G(CN,J,J)
2      IMPLICIT DOUBLE PRECISION(A-H,O-Z)
3      C.....
4      C..... IRWIN'S CONDUCTIVITY FORMULAS.
5      C.....
6      IF (J.J.EQ.1) GO TO 3
7      IF (CN.GT.0.0) A=1.0
8      IF (CN.GT.0.0) B=7.2D-17
9      IF (CN.GT.1.5D-14) A=0.45
10     IF (CN.GT.1.5D-14) B=3.3D-11
11     IF (CN.GT.2.4D-14) A=0.832
12     IF (CN.GT.2.4D-14) B=1.47D-14
13     IF (CN.GT.1.5D-19) A=0.966
14     IF (CN.GT.1.5D-19) B=4.D-17
15     GO TO 5
16     3  IF (CN.GT.0.0) A=1.0
17     IF (CN.GT.0.0) B=2.D-14
18     IF (CN.GT.3.5D-15) A=0.837
19     IF (CN.GT.3.5D-15) B=6.97D-14
20     IF (CN.GT.1.0D-17) A=0.543
21     IF (CN.GT.1.0D-17) B=6.93D-9
22     IF (CN.GT.9.5D-18) A=0.94
23     IF (CN.GT.9.5D-18) B=2.D-14
24     IF (CN.GT.4. D-19) A=0.744
25     IF (CN.GT.4. D-19) B=1.43D-12
26     IF (CN.GT.2.35D-20) A=0.456
27     IF (CN.GT.2.35D-20) B=1.04D-4
28     5  B=B*(CN**A)
29     RETURN
30     END

```

11CRON*505211).OXDATA

```

C.....SUBROUTINE (OXDATA(AMBNT,ORINT,T,H,C,M,KB)
C.....
C.....SUBROUTINE FOR OXIDATION PARAMETERS AND SEGREGATION CO-EFFI.
C.....
C.....
C.....IMPLICIT DOUBLE PRECISION(A-H,O-Z)
C.....INTEGER AMBNT,ORINT
C.....DOUBLE PRECISION KB,H,M1,M3
C.....
C.....IF (AMBNT.EQ.1) GO TO 12
C.....M=4.40277D-10*DEXP(-7945.74/T)
C.....IF (ORINT.EQ.1) C=4.94558D-10*DEXP(-22184.07/T)
C.....IF (ORINT.EQ.2) C=9.13546D-10*DEXP(-21835.313/T)
C.....IF (ORINT.EQ.3) C=1.4060D-10*DEXP(-22396.838/T)
C.....GO TO 14
12 CONTINUE
C.....M=1.58507D-9*DEXP(-13916.6449/T)
C.....IF (ORINT.EQ.1) C=2.0093D-10*DEXP(-24118.98/T)
C.....IF (ORINT.EQ.2) C=4.33277D-10*DEXP(-24551.98/T)
C.....IF (ORINT.EQ.3) C=7.07945D-10*DEXP(-24957.028/T)
14 CONTINUE
C.....M1=33.3*DEXP(-0.52/(KB*T))
C.....M3=20.0*DEXP(-0.52/(KB*T))
C.....IF (ORINT.EQ.1) M=M1
C.....IF (ORINT.EQ.2) M=(M1+M3)/2.0
C.....IF (ORINT.EQ.3) M=M3
C.....RETURN
C.....END

```

1 MICRON=505211).FRONT

```

2      SUBROUTINE FRONT(IMAXI,JMAXI,LI,K,TEMP,DFI,DELT,JSTEP,
3      * KTYPE,KOTI,XDIST)
4      C
5      C
6      C
7      C
8      C
9      C
10     C
11     C
12     C
13     C
14     C
15     C
16     C
17     C
18     C
19     C
20     C
21     C
22     C
23     C
24     C
25     C
26     C
27     C
28     C
29     C
30     C
31     C
32     C
33     C
34     C
35     C
36     C
37     C
38     C
39     C
40     C
41     C
42     C
43     C
44     C
45     C
46     C
47     C
48     C
49     C
50     C
51     C
52     C
53     C

```

SUBROUTINE FRONT(IMAXI,JMAXI,LI,K,TEMP,DFI,DELT,JSTEP,
* KTYPE,KOTI,XDIST)

SUB. FOR CALCULATING CONTOUR FRONT MOVEMENT DATA AND
READING AND WRITING THE SAME ON FILE

IMPLICIT DOUBLE PRECISION(A-H,O-Z)
DIMENSION XFRONT(1), YFRONT(1)
DATA IDOL,IBLNK,14YR/1HS,1H,1H0/
IF(KTYPE.NE.1) GO TO 800

READ FILE

DO 60 KK=1,JSTEP
 READ(9,390) MARK
 IF (MARK.NE.IDOL) GO TO 50
 READ(9,430) TEMP,DFI,DELT
 READ(9,420) MARK
50 READ(9,430) (DUM,LL=1,6)
 READ(9,430) (DUM,LL=1,6)
 READ(9,420) IMAXI,JMAXI,K,LM
60 CONTINUE
 RETURN
800 CONTINUE
 DO 260 LL=1,6
 CONVAL=10.0*FLOAT(20-LL+1)
 XF=CONDEP(IMAXI,JMAXI,0,-JMAXI,0,0,CONVAL)
 YF=CONDEP(IMAXI,JMAXI,-2,0,0,0,CONVAL)
 IF (XF.EQ.0.0) GO TO 250
 XFRONT(LL)=(XF-FLOAT(K))/(XDIST/FLOAT(JMAXI-1))
250 CONTINUE
 IF (YF.EQ.0.0) GO TO 260
 YFRONT(LL)=(YF-FLOAT(JMAXI-1))/FLOAT(JMAXI-1)
260 CONTINUE

STORE CONTOUR FRONT MOVEMENT DATA IF IFILE = 1

MARK=IDOL
IF (KOTI.GT.1) MARK=IBLNK
WRITE(9,390) MARK
IF (KOTI.GT.1) GO TO 270
WRITE(9,430) TEMP,DFI,DELT
MARK=IBLNK
WRITE(9,390) MARK
270 WRITE(9,430) (XFRONT(LL),LL=1,6)
 WRITE(9,430) (YFRONT(LL),LL=1,6)
 WRITE(9,420) IMAXI,JMAXI,K,LM
390 FORMAT(1H0,A6)
400 FORMAT(1H,3F10.1)
420 FORMAT(1H,4F5)
430 FORMAT(1H,6(E14.9,2X))
RETURN
END

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```

80      30 CALL PLOT(XX,19.5*DY,(2)
81      DO 40 I=1,20
82      YY=(I-1)*DY
83      CALL PLOT(XX,YY,3)
84      40 CALL PLOT(14.*DX,YY,12)
85      C *** PUT SYMBOL
86      CALL SYMBOL(0.5,4.7,0.1313,1A,0.0,33)
87      IF(N.EQ.2) IX=IY
88      CALL SYMBOL(1.6,4.45,0.1313,1X,0.0,14)
89      C *** AXES NUMBERS
90      V=-0.2
91      DO 50 J=1,11
92      X=FLOAT(I-1)*2.*DX=-.125
93      VAL=FLOAT(I-1)*TAUM/10.
94      50 CALL NUMBER(X,Y,HRT,VAL,0.0,2)
95      X=-0.5
96      DO 60 J=1,21
97      Y=FLOAT(J-1)*DY=-.043
98      VAL=FLOAT(J-1)*YDMAX/20.
99      60 CALL NUMBER(X,Y,HRT,VAL,0.0,2)
100      CALL SYMBOL(-.75,2.1,0.1313,DISTANCE*.90,.0)
101      CALL SYMBOL(2.1,-.5,0.1313,NORMALIZED TIME - TAU,0.0,21)
102      DO 70 LL=1,4
103      CALL PLOT(0.0,0.0,3)
104      XMOVE=0.
105      CALL PLOT(TAU,XMOVE,2,0)
106      DO 70 HL=1,JSTEP
107      TAUP=TAU(HL)*XMAX/TAUM
108      XMOVE=XFRONT(HL,LL)*YMAX/YDMAX
109      IF(N.EQ.2) YMOVE=YFRONT(HL,LL)*YMAX/YDMAX
110      IF(TAU.GT.0.0.AND.YMOVE.EQ.0.0.AND.N.EQ.2) GO TO 70
111      IF(N.EQ.2) XMOVE=YMOVE
112      IF(XMOVE.LT.0.0) XMOVE=0.0
113      CALL PLOT(TAUP,XMOVE,2,0)
114      70 CONTINUE
115      CALL PLOT(0.0,0.999)
116      80 CONTINUE
117      STOP
118      END

```


1 MICRON=5052(1),SHFILE

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14

C
C
C

SUBROUTINE SHFILE(TIME,DELT,DELY,TEMP,THAX,RS,VJI,VJUNC,0
• JMAX,YDIST,XO,IAHANT)

SUB WRITES SEET RESISTANCE, JUNCTION DEPTH AND INTEGRATED
IMPURITY ON UNIT 14

IMPLICIT DOUBLE PRECISION(A-H,O-Z)

200 WRITE(13,200) JMAX,IAHANT
FORMAT(1H0,8I10)

WRITE(13,100) TEMP,THAX,DELT,DELY,YDIST
100 WRITE(13,100) RS,VJI,VJUNC,0,TIME,XO

FORMAT(1H0,6E15.0)

RETURN
END

41CNON=5052(1).OUTPUT

```

1  SURROITIME OUTPUT(X,Y,IMAXI,JHAXI,K,LM,JJ,TIME,YDIST,
2  *IO,ITIME,XO,PTIME,DTIME,IAMBNT)
3
4  C
5  C
6  C
7  C
8  C
9  C
10  C
11  C
12  C
13  C
14  C
15  C
16  C
17  C
18  C
19  C
20  C
21  C
22  C
23  C
24  C
25  C
26  C
27  C
28  C
29  C
30  C
31  C
32  C
33  C
34  C
35  C
36  C
37  C
38  C
    TRANSIENT DATA PRINT OUT
    IMPLICIT DOUBLE PRECISION(A-H,O-Z)
    COMMON /CON/CB1(4,4)
    DIMENSION X(1),Y(1),ID(15),XO(1)
    IMAX=IMAXI-1
    IMAX2=IMAXI+1
    PRINT 104, IO,ITIME
    PRINT 100, LM,TIME,PTIME,DTIME,K,X(K),IMAXI,X(IMAXI)
    PRINT 101, (N,N=2,IMAXI,2)
    PRINT 102, (X(I),I=2,IMAXI,2)
    PRINT 105
    W1=YDIST-0.45*XO(5)
    DO 2 J=JHAXI,1,-1
    Q=YDIST-Y(J)
    IF(IAMBNT.NE.3) Q=(JHAXI-J)*41./FLOAT(JHAXI-1)
    PRINT 103, Q,(CB1(I,J),I=2,IMAXI,2)
    PRINT 108, (XO(I),I=2,IMAXI,2)
    IF(IAMBNT.NE.3) PRINT 109, W1
109  FORMAT(1H0,10X,'SI FILM' = ,F10.5)
108  FORMAT(1H0,10X,'OXIDE THICKNESS IN CM' = ,F10.13X,11(1PF10.3))
    PRINT 104, JJ
100  FORMAT(1H0,10X,12UTIME STEP = ,14.3X,7HTIME = ,F10.3,
    *5X,ELAPSED TIME IN SEC.11,2X,PREDEP = ,F10.3,2X,DRIVE IN = ,
    * F10.3//
    *10X,OXIDE POSITION//
    *10X,X(1,12,1) = ,E6.2,2X,X(1,12,1) = ,E6.2//)
101  FORMAT(//,1H0,3HI = ,6X,12110)
102  FORMAT(//,1H0,3X,3HX = ,7X,12(1PF10.3))
103  FORMAT(1H,2X,'Y' = ,1PF7.1,2X,11(1PF10.3))
104  FORMAT(//,1H0,'NO. OF ITERATION' = ,15)
105  FORMAT(1H0)
106  FORMAT(1H1,10X,15A4,T98,'TIME',A6)
    RETURN
    END

```

PRY 5052,PLOT-CONTOUR,,SUBION,,TRINAG,,ARC,,XYZ,,PLOT,,CONDEP,,MAIN

11CRON=5052(1).PLOT=CONTOUR

```

1  SUBROUTINE PLYCON(A,CONVAL,NC,IK,JK)
2  C
3  C 190CONCENTRATION PLOT SUBPROGRAM
4  C
5  DIMENSION A(4,4),X(1000,3),Y(1000,3),NV(1000)
6  DIMENSION CS(2,3),CT(2,2,4),OT(2,4),B(4),OS(2,3)
7  DATA ZERO/1.0E-20/
8  DATA ((CS(I,J),J=1,3),I=1,2)/0.5,-1.0,0.5,-0.5,0.0,0.5/
9  DATA ((CT(I,J,K),K=1,4),J=1,2)/1.2/1.0,0.0,-1.0,0.0,n,0.1,n
10  DATA ((OT(I,J),J=1,4),I=1,2)/0.0,0.0,1.0,1.0,0.0,1.0,1.0,0.0/
11  DATA ((OS(I,J),J=1,3),I=1,2)/0.5,1.0,0.0,0.5,0.0,0.0/
12  DATA XMAX,YMAX/8,n,4,n/
13  NCH=NC-1
14  CONTUR=ALOG10(CONVAL)
15  C * RESET PEN TO ORIGIN
16  C * CALL PLOT(0,0,0,0)
17  C * COMPUTE SCALING FACTORS
18  SCALX=XMAX*1.5/(IK-2)
19  SCALY=YMAX/(JK-1)
20  C * START CONTOUR SEARCH
21  NT=0
22  IL=IK-1
23  JL=JK-1
24  DO 50 I=2,IL
25  DO 50 J=1,JL
26  C * LOCATE SQUARE CROSSINGS
27  I1=I-2
28  J1=J-1
29  B(1)=0.25*(ALOG10(A(I,J))+ALOG10(A(I+1,J))+ALOG10(A(I,J+1))+
30  *ALOG10(A(I+1,J+1)))
31  R(1)=10.0*B(1)
32  R(4)=R(1)
33  C * LOCATE TRIANGLES
34  DO 40 K=1,4
35  NP=0
36  GO TO (21,22,23,24),K
37  21 R(2)=A(I+1,J)
38  R(3)=A(I,J)
39  GO TO 30
40  22 R(2)=A(I,J)
41  R(3)=A(I,J+1)
42  GO TO 30
43  23 R(2)=A(I,J+1)
44  R(3)=A(I+1,J+1)
45  GO TO 30
46  24 R(2)=A(I+1,J+1)
47  R(3)=A(I+1,J)
48  GO TO 30
49  C * LOCATE INTERSECTIONS
50  DO 35 M=1,3
51  IF (CONVAL.LT.AMIN1(R(M),B(M+1)).OR.CONVAL.GT.AMAX1(B(M),B(M+1)))
52  *GO TO 35
53  NP=NP+1
54  RB=ALOG10(B(M+1))-ALOG10(R(M))
55  IF (ABS(RB).GT.ZERO) GO TO 33
56  N=0.5
57  GO TO 34
58  33 N=(CONTUR-ALOG10(R(M)))/RB
59  CONTINUE
60  TX=OS(1,M)+CS(1,M)*D
61  TY=OS(2,M)+CS(2,M)*D
62  X(NT+1,NP)=OT(1,K)+CT(1,1,K)*TX+CT(1,2,K)*TY+11
63  Y(NT+1,NP)=OT(2,K)+CT(2,1,K)*TX+CT(2,2,K)*TY+JJ
64  35 CONTINUE
65  IF (NP.LE.1) GO TO 40
66  NT=NT+1
67  NV(NT)=NP
68  40 CONTINUE
69  50 CONTINUE
70  C * SCALE POINTS
71  IF (NT.EQ.0) GO TO 80
72  DO 65 K=1,NT
73  NM=NV(K)
74  DO 65 L=1,NM
75  X(K,L)=X(K,L)*SCALX
76  Y(K,L)=Y(K,L)*SCALY
77  65 CONTINUE
78  C * PLOT CONTOUR
79

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```

DO 71 K=1,NT
NH=NV(K)
CALL PLOT(X(K,1),Y(K,1),3)
IF (MOD(K,10).EQ.0) CALL SYMBOL(X(K,1),Y(K,1),0,10,NCHI,n*0,-1)
DO 71 L=2,NH
CALL PLOT(X(K,L),Y(K,L),2)
IF (NH.EQ.3) CALL PLOT(X(K,1),Y(K,1),2)
71 CONTINUE
C. 71 MOVE PEN TO ORIGIN
80 CALL PLOT(0.0,0.0,1,3)
RETURN
END
  
```

4ICRON=5052(1).YRIDAG

```
1 SUBROUTINE YRIDAG(JF,1)
2 C.....
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18
19
C
  DIMENSION GAMMA(44),BETA(44)
  BETA(JF)=R(JF)
  GAMMA(JF)=D(JF)/BETA(JF)
  JFPI=JF+1
  DO 100 I=JFPI,L
    BETA(I)=B(I)-A(I)*C(I-1)/BETA(I-1)
  100 GAMMA(I)=(D(I)-A(I)*GAMMA(I-1))/BETA(I)
  LAST=L-JF
  V(L)=GAMMA(L)
  DO 200 K=1, LAST
    I=L-K
    V(I)=GAMMA(I)-C(I)*V(I+1)/BETA(I)
  200
  RETURN
  END
```

MICRON=5n52(1).SUBION

```

1 SUBROUTINE SUBION(IMAXI,JMAXI,K,YDIST,CSTOP)
2 C.....
3 C.....
4 C.....
5 C.....
6 C.....
7 C.....
8 C.....
9 C.....
10 C.....
11 C.....
12 C.....
13 C.....
14 C.....
15 C.....
16 C.....
17 C.....
18 C.....
19 C.....
20 C.....
21 C.....
22 C.....
23 C.....
24 C.....
25 C.....
26 C.....

```

SUBROUTINE FOR GENERATING ION IMPLANT DATA

IMPLICIT DOUBLE PRECISION(A-H,O-Z)

COMMON /CON/CR1(4,4)

DIMENSION Y(1)

ISS=0

JH=JMAXI/2

IF(Y(JH).LT.1.D-3) ISS=1

READ 100, CHAX,RP,DRP,VOLT

FORMAT(5E15.6,F10.5)

PRINT 200, CHAX,RP,DRP,VOLT,CSTOP

200 FORMAT(7//1H0,'CHAX = ',E10.5,' CM=3',3X,'RP = ',E10.5,' MICRON',

1H,'DRP = ',E10.5,' MICRON',71H,'ION IMPLANTATION WITH

1H,'NORON IMPLANT AT',F10.5,' KEV',5X,'CSTOP = ',E15.6)

IF(ISS.EQ.1) RP=RP/2

IF(ISS.EQ.1) DRP=DRP/2

DO 1 J=1,JMAXI

1 CB1(1,J)=CHAX*DEXP(-0.5*((YDIST-Y(J)-RP)/DRP)**2)

DO 2 J=1,JMAXI

DO 3 I=2,K

3 CB1(I,J)=CB1(1,J)

2 CONTINUE

RETURN

END

MICRON=5n52(1).ABC

```

1 SUBROUTINE ABC(IMAXI,JMAXI,X,Y,LM,TIME,K,DFI,TEMP,TMAX,KOTI,XO,
2 YDIST,IAHNT)
3 C.....
4 C.....
5 C.....
6 C.....
7 C.....
8 C.....
9 C.....
10 C.....
11 C.....
12 C.....
13 C.....
14 C.....
15 C.....
16 C.....
17 C.....
18 C.....
19 C.....
20 C.....
21 C.....
22 C.....
23 C.....
24 C.....
25 C.....
26 C.....
27 C.....
28 C.....
29 C.....
30 C.....
31 C.....
32 C.....
33 C.....
34 C.....
35 C.....
36 C.....

```

SUBROUTINE WRITES TRANSIENT DATA ON DATA FILE ON UNIT 11

DOUBLE PRECISION CR1,X,Y,TIME,TEMP,TMAX,DFI,XO,YDIST

COMMON /CON/CR1(4,4)

DIMENSION XO(1)

DIMENSION X(1),Y(1)

DATA IDOL,IBLNK/14,1H /

KOTI=KOTI+1

MARK=IDOL

IF(KOTI.GT.1) MARK=IBLNK

WRITE(11,400) MARK

400 FORMAT(1H0,A6)

IF(KOTI.GT.1) GO TO 2

WRITE(11,100) DFI,TMAX,TEMP,YDIST

WRITE(11,200) K,IMAXI,JMAXI,IAHNT

200 FORMAT(1H,8110)

WRITE(11,100) (X(I),I=2,IMAXI)

WRITE(11,100) (Y(I),I=1,JMAXI)

MARK=IBLNK

WRITE(11,400) MARK

2 CONTINUE

WRITE(11,200) LM

WRITE(11,100) TIME

DO 1 J=JMAXI,1,-1

1 WRITE(11,100) (CR1(I,J),I=2,IMAXI)

WRITE(11,100) (XO(I),I=2,IMAXI)

100 FORMAT(1H,5E15.9)

PRINT 300, KOTI

300 FORMAT(1H,10X,'KOTI = ',110/)

RETURN

END

ORIGINAL PAGE IS
OF POOR QUALITY

4ICRON=50S2(1),XYZ

```

1 SUBROUTINE XYZ(IMAXI,JMAXI,X,Y,LM,TIME,K,DFI,TEMP,THAX,KOTI,XO,
2   YDIST,IAMBNT)
3 C.....
4 C
5 C SUBROUTINE READS THE TRANSIENT DATA FILE ON UNIT 11
6 C
7 C DOUBLE PRECISION (BI,X,Y,TIME,TEMP,THAX,DFI,XO,YDIST
8 COMMON /CON/CBI(64,64)
9 DIMENSION XO(1)
10 DIMENSION X(1),Y(1)
11 DATA 100L,10LKN/100,10 /
12 DO 3 KLM=1,KOTI
13 READ(11,400) MARK
14 IF(MARK.NE.100L) GO TO 5
15 READ(11,100) DFI,THAX,TEMP,YDIST
16 READ(11,200) K,IMAXI,JMAXI,IAMBNT
17 100 FORMAT(1H,5E15.9)
18 200 FORMAT(1H,8I10)
19 READ(11,100) (X(I),I=2,IMAXI)
20 READ(11,100) (Y(I),I=1,JMAXI)
21 READ(11,100) MARK
22 5 CONTINUE
23 READ(11,200) LM
24 READ(11,100) TIME
25 DO 1 J=JMAXI,1,-1
26 1 READ(11,100) (CBI(1,J),I=2,IMAXI)
27 READ(11,100) (XO(I),I=2,IMAXI)
28 3 CONTINUE
29 400 FORMAT(1H0,A6)
30 C APPLY PERIODIX B.C.
31 IMAX2=IMAXI+1
32 IMAX=IMAXI-1
33 DO 7 J=1,JMAXI
34 7 CBI(1,J)=CBI(3,J)
35 CBI(IMAX2,J)=CBI(1,IMAX,J)
36 RETURN
37 END

```

MICRON=SnS2(1).PLOT

```

SUBROUTINE PLOT(CS,IMAXI,JMAXI,N)
.....
SUBROUTINE PLOTS THE TWO DIMENSIONAL PROFILE
IN THE OUTPUT PRINTOUT IF IPLOT = 1
.....
DOUBLE PRECISION CBI,CS
COMMON /CON/CBI(44,44)
DIMENSION SYMBL(21),ULINE(43)
DIMENSION IX(32)
DATA SYMBL/1HA,1H ,1HR,1H ,1HC,1H ,1HD,1H ,1HE,1H ,1HF,1H ,
1HG,1H ,1HH,1H ,1HI,1H ,1HJ,1H ,1HK,1H /
DATA DOT,STAR/1H ,1H,2,KP/21/
DATA IX/6,1H ,1H,1H ,1HA,1HX,1HI,1HS,20,1H /
IMAX=IMAXI-1
PRINT 11
AT=ALOG10(2.2D11)
FACT=(ALOG10(CS)-AT)/(FLOAT(KP-1))
K=0
DO 2 J=JMAXI,1,-1
DO 1 I=2,IMAXI
IF(CBI(I,J).LE.0.0) GO TO 3
K=(IALOG10(CBI(I,J))-AT)/FACT+1.0
3 CONTINUE
IF(K.LT.1) ULINE(I)=DOT
IF(K.GE.1.AND.K.LE.KP) ULINE(I)=SYMBL(K)
1 IF(K.GT.KP) ULINE(I)=STAR
2 PRINT 10,IX(I), (ULINE(I),I=2,IMAXI),(ULINE(I),I=IMAX,2,-1)
PRINT 12
PRINT 13
PRINT 14,SYMBL(KP),CS
KD=KP-1
DO 4 I=KD,1,-1
CBL=10.00*((I-1)*FACT+AT)
CBH=10.00*(I*FACT+AT)
4 PRINT 15,SYMBL(I),CBH,CBL
PRINT 16
10 FORMAT(1H ,A1,IX,1H,70A1)
11 FORMAT(1H ,1IMPURITY CONCENTRATION PROFILE//
12 1HO,41(1H) ,///)
13 FORMAT(1H ,IX,50(1H-1)//1H ,15X,1X AXIS//
14 /,1HO,1SYMBOLIC REPRESENTATION OF CONCENTRATION RANGES,
15 //1HO,1T10,1SYMBOL,1T30,1CONCENTRATION RANGE//1H ,1T10,6(1H-1),T30,
16 19(1H-1)/ 1HO,1T13,1H,1T29,1ABOVE SURFACE CONC.//
14 FORMAT(1H ,T13,A1,T29,1AT CS = ,F10.3)
15 FORMAT(1H ,T13,A1,3X,1LESS THAN,1E10.3,3X,1GREATER THAN OR EQUAL,1
16 1E10.3)
16 FORMAT(1H ,T13,1H,1T29,1BELOW 1.0DOE11)
RETURN
END

```


MICRON=505211).CONDEP

```

1  FUNCTION CONDEP(M,N,I,J,MIN,MAX,CONVAL)
2  * LOCATES CONCENTRATION CONTOURS ALONG EITHER
3  * A VERTICAL OR HORIZONTAL GRID LINE. EITHER
4  * LINEAR OR LOGRITHMIC INVERSE INTERPOLATION
5  * CAN BE USED.
6
7  *
8  *
9  *
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```

A - ARRAY BEING CONTOURED (DIMENSIONED (M,N) IN CALLING PROGRAM)
 I,J - NON-ZERO VALUE SPECIFIES GRID LINE TO BE CONTOURED. POSITIVE VALUE FOR LINEAR INTERPOLATION, NEGATIVE FOR LOGRITHMIC INTERPOLATION. EITHER I OR J MUST BE ZERO.
 CONVAL - CONTOUR VALUE
 MIN, - MINIMUM AND MAXIMUM SUBSCRIPTS OF GRID LINE TO BE CONTOURED. (MAY BE ZERO IF ENTIRE GRID LINE IS TO BE CONTOURED.)
 MAX -
 CONDEP - POSITION OF CONVAL ON GRID LINE. IF CONVAL IS OUT OF RANGE OF GRID LINE VALUES CONDEP RETURNS A VALUE OF ZERO.

```

1  IMPLICIT DOUBLE PRECISION(A-H,O-Z)
2  COMMON /CON/A(64,64)
3  DO 100 I=1,M
4  DO 100 J=1,N
5  IF (A(I,J).LT.1.0D-100) A(I,J)=1.0D-100
6  ILOG=1
7  IF (I.NE.0) GO TO 10
8  JINC=1
9  JMIN=MIN
10 JMAX=MAX-1
11 IF (MIN.EQ.0) JMIN=1
12 IF (MAX.EQ.0) JMAX=N-1
13 IF (J.LT.0) ILOG=-1
14 JINC=0
15 JMIN=ABS(J)
16 JMAX=JMIN
17 GO TO 20
18
19 10 CONTINUE
20 JINC=1
21 JMIN=MIN
22 JMAX=MAX-1
23 IF (MIN.EQ.0) JMIN=1
24 IF (MAX.EQ.0) JMAX=N-1
25 IF (I.LT.0) ILOG=-1
26 JINC=0
27 JMIN=ABS(I)
28 JMAX=JMIN
29
30 20 CONTINUE
31 CONDEP=0.0
32 DO 45 II=JMIN,JMAX
33 DO 40 JJ=JMIN,JMAX
34 IF (CONVAL.LT.AMIN(A(II,JJ),A(II+IINC,JJ+JINC)))
35 1.0R.CONVAL.GT.AMAX(A(II,JJ),A(II+IINC,JJ+JINC))
36 260 TO 40
37 IF (ILOG.LT.0) GO TO 30
38 CONDEP=((CONVAL-A(II,JJ))/(A(II+IINC,JJ+JINC)-A(II,JJ)))
39 1.FLOAT(II+IINC+JJ+JINC)
40 RETURN
41
42 30 CONTINUE
43 CONLOG=ALOG10(CONVAL)
44 CONDEP=((CONLOG-ALOG10(A(II,JJ)))/(ALOG10(A(II+IINC,JJ+JINC))-
45 1.0LOG10(A(II,JJ))))+FLOAT(II+IINC+JJ+JINC)
46 RETURN
47
48 40 CONTINUE
49 45 CONTINUE
50 RETURN
51 END

```

PROCSIM 11

SOLUTION OF DIFFUSION PROBLEM FOR SILICON ON SAPPHIRE
*** NORMALIZED SOLUTION ***

DATA IS READ FROM DECK IN FOLLOWING SEQUENCE:

FIRST CARD:

LIST - # OF TIME STEPS TO BE SKIPPED WHILE PRINTING
 IFILE - PUT 1 TO WRITE ON FILE AND ALSO TO LOCATE
 CONTOUR POSITION, CONTOUR FRONT MOVEMENT DATA IS
 WRITTEN ON UNIT 9 AND CONCENTRATION PROFILE IS
 WRITTEN ON UNIT 11.
 LFILE - # OF TIME STEPS TO BE SKIPPED WHILE WRITING ON FILE
 IPLOT - PUT 1 TO PLOT PROFILE PRINT OUT
 IREAD - PUT 1 TO READ DATA FROM FILE
 - PUT 2 TO READ ION IMPLANT DATA AND TO
 DO REDISTRIBUTION.
 JSTEP - # OF DATA STEPS TO BE READ FROM FILE IF IREAD = 1
 IMAXI, JMAXI - # OF GRID POINTS IN X AND Y DIRECTIONS
 RESPECTIVELY, CHECK DIMENSION BEFORE CHANGING
 FORMAT FIELD = 8110

SECOND CARD:

JSTP - PUT 0 IF CONST. SOURCE DIFF. IS DESIRED.
 - PUT 1 IF REDISTRIBUTION IS DESIRED.
 - PUT 2 IF TWO-STEP DIFF. IS DESIRED
 ORINT - PUT 1 FOR 100 CRYSTAL ORIENTATION
 - PUT 2 FOR 110 CRYSTAL ORIENTATION
 - PUT 3 FOR 111 CRYSTAL ORIENTATION
 AMBNT - PUT 1 FOR DRY OXYGEN
 - PUT 2 FOR STEAM
 - PUT 3 FOR NITROGEN
 FIELD 3110

THIRD CARD:

CSUR - SUBSTRATE DOPING/1.E15
 CS - SURFACE CONCENTRATION/1.E18
 TEMP - TEMPERATURE IN DEG. CENT.
 THAX - NORMALIZATION TIME IN SECOND
 THIS HAS NO EFFECT IF LAMDA IS SPECIFIED AS DATA
 XDIST, YDIST - WIDTH AND THICKNESS (IN MICRON) OF THE TWO
 DIMENSIONAL REGION IN QUESTION
 OXTHIC - WIDTH (IN MICRON) OF THE OXIDE IN THE REGION
 DELT - NORMALIZED TIME STEP
 FORMAT FIELD = 8710.3

FORTH CARD:

INTYPE - SPECIFY TYPE OF IMPURITY BY PUTTING N OR P
 NO SPEC. IS NECESSARY IF IT IS BORON
 IMPUTY - PUT BORON, ARSFNIC, PHOSPHOROUS OR ANY
 OTHER NAME.
 EA - ACTIVATION ENERGY OF THE DIFFUSION
 IF BLANK AND BORON DIFF., DATA IS SUPPLIED INTERNALLY
 DI - DIFFUSIVITY CONST. OF THE IMPURITY.
 IF BLANK AND BORON DIFF., DATA IS SUPPLIED INTERNALLY
 FIELD A4.4A4.2F10.3

FIFTH CARD:

ID - IDENTIFICATION COMMENT TO BE PRINTED ON TOP OF
 PROFILE PRINT OUT
 ITEST - PUT 0 TO READ LAMDA FROM DATA DECK
 CSTOP - CONCENTRATION/1.E15 AT WHICH SIMULATION STOPS
 WHEN THE LEFT END CORNER OF SILICON AND SAPPHIRE
 INTERFACE REACHES THIS VALUE (DURING PREDEP)
 FORMAT FIELD = 15A4.15.F15.9

SIXTH CARD (USE IF JSTP=0):

ROTEMP - REDISTRIBUTION TEMPERATURE
 ROTMAX - REDISTRIBUTION NORM. TIME
 REDISTRIBUTION FINAL TIME IS 1.
 MODLT - REDISTRIBUTION NORM. TIME STEP.
 XOA - REDISTRIBUTION INITIAL OXIDE THICKNESS IN CM

```

80 C** WHERE SURF. CONC. WAS CS
81 C** XON = REDISTRIBUTION INITIAL OXIDE THICKNESS IN CM
82 C** WHERE SURF. WAS THE THICK OXIDE
83 C** CH = SEGREGATION COEFFICIENT, GENERATED INTERNALLY IF
84 C** IMPURITY IS BORON AND NO VALUE IS GIVEN
85 C** FIELD 6F10.3
86 C**
87 C** SEVENTH CARD (USE WHEN ITEST=0)
88 C** LAMDA = LAMDA**2/1.E-3
89 C** FORMAT F10.3
90 C**
91 C** EIGHTH CARD (USE IF IREAD=2)
92 C** ION IMPLANTATION DATA
93 C** CHAX = MAX. CONCENTRATION
94 C** RP = RANGE OF DISTRIBUTION, MEAN VALUE (IN MICRON )
95 C** DRP = STRAGGLE, STANDARD DEVIATION, (IN MICRON )
96 C** VOLT = IMPLANTATION ENERGY LEVEL IN KEV
97 C** FIELD 3E15.6,F10.5
98 C**
99 C*****
100 C
101 C IMPLICIT DOUBLE PRECISION (A-H,O-Z)
102 C INTEGER ORINT,AMBNT
103 C DOUBLE PRECISION KB,N1,LAMDA
104 C COMMON /TRI/ A(64),B(64),D(64),E(64),V(64)
105 C COMMON /CON/ CB1(64,64)
106 C DIMENSION X(64),Y(64),CB(64,64),CB2(64,64),G(64,64),ID(16)
107 C DIMENSION IMTYPE(1),IMPUTY(4),IRON(4)
108 C DIMENSION XOLAST(64),XO(64),DRHXO(64),VP(64)
109 C DIMENSION IMAT(2),IORNT(1),IDOX(2),INIT(2),ISTH(1)
110 C
111 C
112 C
113 C
114 C
115 C
116 C
117 C
118 C
119 C
120 C
121 C
122 C
123 C
124 C
125 C
126 C
127 C
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159 C

```

WHERE SURF. CONC. WAS CS
XON = REDISTRIBUTION INITIAL OXIDE THICKNESS IN CM
WHERE SURF. WAS THE THICK OXIDE
CH = SEGREGATION COEFFICIENT, GENERATED INTERNALLY IF
IMPURITY IS BORON AND NO VALUE IS GIVEN
FIELD 6F10.3

SEVENTH CARD (USE WHEN ITEST=0)
LAMDA = LAMDA**2/1.E-3
FORMAT F10.3

EIGHTH CARD (USE IF IREAD=2)
ION IMPLANTATION DATA
CHAX = MAX. CONCENTRATION
RP = RANGE OF DISTRIBUTION, MEAN VALUE (IN MICRON)
DRP = STRAGGLE, STANDARD DEVIATION, (IN MICRON)
VOLT = IMPLANTATION ENERGY LEVEL IN KEV
FIELD 3E15.6,F10.5

.....

IMPLICIT DOUBLE PRECISION (A-H,O-Z)
INTEGER ORINT,AMBNT
DOUBLE PRECISION KB,N1,LAMDA
COMMON /TRI/ A(64),B(64),D(64),E(64),V(64)
COMMON /CON/ CB1(64,64)
DIMENSION X(64),Y(64),CB(64,64),CB2(64,64),G(64,64),ID(16)
DIMENSION IMTYPE(1),IMPUTY(4),IRON(4)
DIMENSION XOLAST(64),XO(64),DRHXO(64),VP(64)
DIMENSION IMAT(2),IORNT(1),IDOX(2),INIT(2),ISTH(1)

DEFINE COMPUTING FUNCTIONS

RHS(G,G1,G3,C10,CND,C20)=CND*G*(G1+C20*G3*C10)
RATIO(C,CSUR,N1)=(C-CSUR)/(2.*N1)
ROOT(RATIO)=DSQRT((RATIO**2)+1.0)
FUI(RATIO,ROOT)=((RATIO+ROOT)**2)/ROOT
CALL ERTRAN (9,DATE,TIME)

READ SIMULATION INITIAL DATA

READ 360,LIST,IFILE,(FILE,IPLOY,IREAD,JSTEP,IMAXI,JMAXI
READ 360,JSTEP,ORINT,AMBNT
IF (IREAD.EQ.2) JSTEP=1
READ 370,CSUB,CS,TEMP,THAX,XDIST,YDIST,OXTHIC,DELT
READ 320,IMTYPE,IMPUTY,EA,DI
READ 380,ID,ITEST,CSTOP
IF (JSTEP.GT.0) READ (5,370,ERR=310) RDTEMP,RDTHAX,RDDLT,XOA,XON,CM
IF (ITEST.EQ.0) READ (5,370,ERR=310) LAMDA

DEFINE DATA:

KB = ROLTZMANN'S CONSTANT
JLIM = # OF ALLOWABLE ITERATIONS
DVLIM = ALLOWABLE ERROR IN CONVERGENCE
TIMAX = NORMALIZED TIME AT WHICH SIMULATION STOPS
EAB AND DIB = BORON DIFFUSIVITY DATA

DATA EAB,DIB /3.59D0,1.17D0/
DATA IBRON /4HBORO,4HN .4H .4H /
DATA NYP,IPT /1HN,1HP/
DATA KB /8.616D-5/
DATA JLIM,DVLIM /60,1.D-6/,TIMAX /1.00/
DATA IDOX/6HDY OX,6HYGEN /
DATA INIT/6HNITROG,6HFN /
DATA ISTH/6HSTEAM /

IF (IMPUTY.EQ.IRON) IMTYPE=IPT
IER=0
IF (JSTEP.EQ.1.AND. IREAD.EQ.0) IER=1
IF (IMPUTY.NE.IRON.AND.EA.EQ.0.00) IER=1
IF (IMPUTY.NE.IRON.AND.DI.EQ.0.00) IER=1
IF (IER.EQ.1) PRINT 450
IF (IER.EQ.1) GO TO 310
IF (IMTYPE.EQ.IPT) ITYPE=0
IF (IMTYPE.EQ.NYP) ITYPE=1
IF (IMPUTY.EQ.IRON.AND.EA.EQ.0.00) EA=EAB
IF (IMPUTY.EQ.IRON.AND.DI.EQ.0.00) DI=DIB
PRINT 410, ID
PRINT 330, IMPUTY,IMTYPE

```

160 NAMELIST /PUT/ LIST,IFILE,LFILE,IPLOT,IHEAD,JSTEP,IMAX1,IMAX2,JSTEP
161 1,ORINT,AMNT,CSUB,CS,TEMP,THAX,KDIST,YDIST,OXTHIC,DELT,CA,DI,ITEST
162 2,CSTOP,LAMDA,NOTEMP,NOTHAX,NDOLT,XOA,XOB,CH,JLIM,DVLIM,TMAX
163 WRITE (4,PUT)
164
165 REFORMATION OF COMPUTING, GEOMETRIC AND PHYSICAL PARAMETERS
166
167 IF (JSTEP.EQ.0.OR.JSTEP.GT.1) ICOND=1
168 IF (ICOND.EQ.1) AMNT=3
169 IF (AMNT.NE.3) XDIST=XDIST*1.0-4
170 IF (AMNT.NE.3) YDIST=YDIST*1.0-4
171 IF (AMNT.NE.3) OXTHIC=OXTHIC*1.0-4
172 JMAX=JMAX1-1
173 KOT=0
174 IMAX=IMAX1-1
175 IMAX2=IMAX1+1
176 IF (IMAX1.GT.3) GO TO 4
177 DELX=4.0
178 IF (AMNT.NE.3) DELX=6.0-4
179 GO TO 4
180 5 DELX=XDIST/FLOAT(IMAX2-3)
181 6 DELY=YDIST/FLOAT(JMAX)
182 CSUB=CSUB*1.015
183 CSTOP=CSTOP*1.015
184 LAMDA=LAMDA*1.0-3
185 CS=CS*1.018
186 T=TEMP+273.
187 WINDO=(XDIST-OXTHIC)*1.0-5
188 CH=CH
189 CH=1.0
190 THX=THAX
191 IF (AMNT.EQ.1) IMAT(1)=IDOX(1)
192 IF (AMNT.EQ.1) IMAT(2)=IDOX(2)
193 IF (AMNT.EQ.2) IMAT=ISTM
194 IF (AMNT.EQ.3) IMAT(1)=INIT(1)
195 IF (AMNT.EQ.3) IMAT(2)=INIT(2)
196 IF (ORINT.EQ.1) IORNT=100
197 IF (ORINT.EQ.2) IORNT=110
198 IF (ORINT.EQ.3) IORNT=111
199
200 CALCULATE DISTANCE X AND Y
201
202 DO 10 I=2,IMAX1
203   X(I)=(I-2)*DELX
204   IF (X(I).LE.WINDO) K=1
205 DO 20 J=1,JMAX1
206   Y(J)=(J-1)*DELY
207 DO 30 I=2,IMAX1
208   XOLAST(I)=XOA
209 DO 31 J=JMAX1,1,-1
210   YP(J)=(JMAX1-J)*(1./FLOAT(JMAX1))
211
212 SPECIFY PREDEF CONDITIONS
213
214 DO 40 I=1,IMAX2
215 DO 40 J=1,JMAX1
216   CR(I,J)=0.0
217   CR1(I,J)=0.0
218   CR2(I,J)=0.0
219 DO 50 I=2,K
220   CR(I,JMAX1)=CS
221   CR1(I,JMAX1)=CS
222   CR2(I,JMAX1)=CS
223 TIME=0.0
224 LM=0
225
226 SPECIFY INITIAL PROFILE
227
228 IF (IREAD.EQ.2) CALL SUBION(IMAX1,JMAX1,K,Y,YDIST,CSTOP)
229 IF (IREAD.EQ.1) CALL XYZ (IMFI,JMFI,X,Y,LM,TIME,KA,DFA,TMP,TMX,JQ
230 ITEMP,XOLAST,YDIST,AMNT)
231 IF (IREAD.EQ.1) TMAX=TIME+1.0
232 STIME=TIME
233 IF (JSTEP.EQ.1) ICOND=2
234
235 HEAD CONTOUR FRONT MOVEMENT FROM DATA FILE IF IREAD = 1
236
237 IF (IREAD.EQ.1) CALL FRONT (IMI,JMI,LA,KC,TMPR,DFA,DLT,LM,I,KOTI,X
238 IDIST)
239 IF (IREAD.EQ.1) PRINT 430, LM,TIME,TMP,DFA,TMX,IMFI,JMFI,KA

```

```

240 IF (IREAD.EQ.1) PRINT 440, TMR,DFB,LA,IMI,JMI
241 IF (IREAD.NE.1) GO TO 60
242 IF (IMF1.NE.IMAX1.OR.IMF1.NE.JMAX1.OR.KA.NE.K) IER=1
243 IF (IMI.NE.IMAX1.OR.JMI.NE.JMAX1.OR.KC.NE.K.OR.LA.NE.LM) IER=1
244 IF (IER.EQ.1) PRINT 450
245 IF (IER.EQ.1) GO TO 310
246
247 C
248 C
249 C
250 C
251 C
252 C
253 C
254 C
255 C
256 C
257 C
258 C
259 C
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301 C
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307 C
308 C
309 C
310 C
311 C
312 C
313 C
314 C
315 C
316 C
317 C
318 C
319 C

```

```

IF (IREAD.EQ.1) PRINT 440, TMR,DFB,LA,IMI,JMI
IF (IREAD.NE.1) GO TO 60
IF (IMF1.NE.IMAX1.OR.IMF1.NE.JMAX1.OR.KA.NE.K) IER=1
IF (IMI.NE.IMAX1.OR.JMI.NE.JMAX1.OR.KC.NE.K.OR.LA.NE.LM) IER=1
IF (IER.EQ.1) PRINT 450
IF (IER.EQ.1) GO TO 310

START SIMULATION STEP

60 IF (ICOND.EQ.1) GO TO 70
KOT1=0
TEMP=RDTEMP
T=TEMP+273.
DELT=RDDELT
TMAX=RDTHAX
IF (AMRNT.NE.3) DELT=DELT+TMAX
IF (AMRNT.NE.3) TMAX=TMAX
TIME=0.
70 CONTINUE

CALCULATE NI
TMAX=TMAX-DELT
CALL PARAM (NI,T)
OF=D1*DEXP(-EA/(K*OT))
IF (ITEST.NE.0) DFI=OF*TMAX/((VDIST+1.D-4)**2)
IF (AMRNT.NE.3) DFI=OF
IF (ITEST.EQ.0) DFI=LAMDA
IF (ICOND.EQ.1) PRINT 340
IF (ICOND.EQ.2) PRINT 350
PRINT 390, NI,OF
PRINT 420, IMPUTY,TEMP,DFI,TMAX

P=(DFI*DELT)/(DELY**2)
Q=(DFI*DELT)/(DELY**2)

PRINT INITIAL PROFILE
CALL OUTPUT (X,Y,TMAX,JMAX,K,LH,JJ,TIME,YDIST,IO,ITIME,XOLAST,
* PTIME,DTIME,AMRNT)
IF (IREAD.EQ.2.AND.IFILE.EQ.1) CALL ARC (IMAX1,JMAX1,X,Y,LH,TIME,K
1,DFI,TEMP,TMAX,KOT1,XOLAST,YDIST,AMRNT)
AM=1.0
CC=1.0
RB=1.0
IF (ICOND.NE.1) CALL OXDATA (AMRNT,ORINT,T,BR,
ICC,AM,KB)
IF (ICOND.EQ.2.AND.GH.EQ.0) CH=AM
IF (ICOND.EQ.2.AND.GH.NE.0) CH=GM
IF (ICOND.EQ.2) PRINT 421, IMRT,IORNT,BR,CC,CH

START TIME STEP LOOP

80 LH=LH+1

STORE N TH. RESULT FOR R.H.S.,WILL NOT BE CHANGED DURING ITER.

TIME=TIME+DELT
IF (ICOND.EQ.1) STIME=TIME
PTIME=TMX*STIME
IF (ICOND.EQ.2) PTIME=TMX
DTIME=RDTHAX*(TIME-STIME)
IF (AMRNT.NE.3) DTIME=TIME
DO 90 I=1,IMAX2
DO 90 J=1,JMAX1
90 CR2(I,J)=CB1(I,J)
IF (ICOND.EQ.1) GO TO 110

CALCULATE OXIDE THICKNESS
IF (AMRNT.NE.3) GO TO 95
DO 94 I=2,IMAX1
94 XO(I)=XOLAST(I)
GO TO 110
95 PS=RB*DELT
QS=RR/CC
DO 100 I=2,IMAX1
XO(I)=XOLAST(I)+PS/12.*XOLAST(I)+QS)
100 ORRXO(I)=(XO(I)-XOLAST(I))/DELT
XO(I)=XO(2)

```

```

370 IF (YDIST-0.45*XN(1)).LT.0.1D 4) GO TO 370
371 CONTINUE
372 DELY=(1./FLOAT(JMAX))*(YDIST-0.45*XOLAST(2))
373 IF (AMNT.NE.3) P=(DF1*DELT)/(DELY*2)
374 JJ=0
375 JH=0
376
377 C
378 C START ITERATION LOOP
379 C
380 C
381 120 JJ=JJ+1
382 IF (JJ.GT.JLIM) PRINT 400, CTER
383 IF (JJ.GT.JLIM) GO TO 290
384
385 C
386 C TRANSFER SOLN. VECTOR FROM LAST ITER. FOR CAL. OF G
387 C
388 C
389 DO 130 I=1,IMAX2
390 DO 130 J=1,JMAX1
391 CR(I,J)=CR(I,J)
392
393 C
394 C CAL. G
395 C
396 DO 140 I=1,IMAX2
397 DO 140 J=1,JMAX1
398 RA=RATIO(CR(I,J),CSUB,N1)
399 RO=ROOT(RA)
400 G(I,J)=FU(RA,RO)
401
402 C
403 C SOLVE SYSTEM IN Y DIRECTION
404 C
405 C
406 DO 220 I=2,IMAX1
407
408 C
409 C CALCULATE THE COEFF. IN Y DIRECTION
410 C
411 C
412 SR=0.
413 DO 150 J=2,JMAX
414 G1=(G(I,J)+G(I+1,J))/2.0
415 G2=(G(I,J)+G(I,J+1))/2.0
416 G3=(G(I,J)+G(I-1,J))/2.0
417 G4=(G(I,J)+G(I,J-1))/2.0
418 IF (AMNT.EQ.3) GO TO 151
419 SR=0.45*DRRXO(1)*(YF(J)-1.0)*DELT/DELY
420
421 151 CONTINUE
422 A(J)=-P*G4
423 R(J)=1.+Q*(G1+G3)+P*(G2+G4)+SR
424 D(J)=-P*G2-SR
425
426 150 E(J)=RHS(Q,G1,G3,CR(I-1,J),CR2(I,J),CR(I+1,J))
427
428 C
429 C PUT BOUNDARY CONDITION ON Y AXIS
430 C
431 C
432 R(2)=A(2)+B(2)
433 A(2)=0.0
434 IF (ICOND.NE.1) GO TO 170
435 IF (I.GT.K) GO TO 160
436 E(JMAX)=E(JMAX)-D(JMAX)*CS
437 D(JMAX)=0.0
438 GO TO 180
439
440 160 CONTINUE
441 B(JMAX)=B(JMAX)+D(JMAX)
442 D(JMAX)=0.0
443 GO TO 180
444
445 170 IF (AMNT.EQ.3) DRRXO(1)=0.
446 HA=-DELY*(1./CH-0.45)*DRRXO(1)
447 HR=2.*DF1
448 HK1=HA/(HR*G(I,JMAX))
449 HK2=HA/(HR*G(I,JMAX))
450 B(JMAX)=B(JMAX)+((1.+HK2)/(1.-HK1))*D(I,JMAX)
451 D(JMAX)=0.
452
453 180 CONTINUE
454
455 C
456 C CALL TRIDAG (2,JMAX)
457 C
458 C
459 C CONVERT MATRIX SOLUTION
460 C
461 C
462 DO 190 J=2,JMAX
463 CR(I,J)=V(J)
464
465 190 CONTINUE
466
467 C
468 C PUT BOUNDARY VALUES IN Y
469 C
470 C
471 CR(I,1)=CR(I,2)

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400 IF (ICOND.NE.1) GO TO 210
401 IF (1.GT.K) GO TO 200
402 CR1(1,JMAX1)=CS
403 GO TO 220
404 CB1(1,JMAX1)=CR1(1,JMAX1)
405 GO TO 220
406
407 210 CONTINUE
408 CB1(1,JMAX1)=(1.+HX2)/(1.+HX1)*CB1(1,JMAX1)
409 IF (CR1(1,JMAX1).LT.1.E-300) CR1(1,JMAX1)=1.E-300
410 220 CONTINUE
411
412 PUT BOUNDARY VALUES IN AXIS X (PERIODIC BOUNDARY)
413
414 DO 230 J=1,JMAX1
415 CR1(1,J)=CB1(1,J)
416 230 CB1(IMAX2,J)=CR1(IMAX,J)
417
418 CHECK FOR CONVERGENCE
419
420 IF (JJ.EQ.1) GO TO 120
421 ICK=0
422 DO 240 I=1,IMAX1
423 DO 240 J=1,JMAX1
424 IF (CB1(1,J).LE.0.0) GO TO 240
425 CTEST=DABS((CR1(1,J)-CB1(1,J))/CB1(1,J))
426 IF (CTEST.LE.OVLIM) GO TO 240
427 CTER=DHAX1(CTEST,CTER)
428 ICK=1
429 240 CONTINUE
430 IF (ICK.NE.0) GO TO 120
431 JH=JH+1
432 DO 241 I=1,IMAX1
433 DO 241 J=1,JMAX1
434 241 IF (CB1(1,J).LT.0.0) CB1(1,J)=CB1(1,J)
435 IF (JH.EQ.1) GO TO 120
436
437 PRINT RESULTS
438
439 IS=LH/LIST*LIST-LM
440 IF (IS.EQ.0) GO TO 250
441 IF (TIME.GE.TIMAX.AND.CS.NE.0.0) GO TO 260
442 IF (CR1(2,1).GE.CSTOP.AND.ICOND.EQ.1) GO TO 260
443 IF (CB1(2,1).GE.CSTOP.AND.CS.EQ.0.0.AND.JSTEP.EQ.1) GO TO 260
444 GO TO 260
445 250 CALL OUTPUT (X,Y,IMAX1,JMAX1,K,LH,JJ,TIME,YDIST,IN,TIME,XO,
446 * PTIME,DTIME,AMNT)
447 CALL SHREJN (CSUR,YDIST,JMAX1,Y,TIME,DELT,DELT,TEMP,THAX,IFILE,ITY
448 IPE,AMNT,XO(2))
449 IF (IPLOT.NE.1) GO TO 260
450 CALL PLOT (CS,IMAX1,JMAX1,K)
451
452 STORE TRANSIENT DATA
453
454 260 IF (IFILE.EQ.0) GO TO 270
455 IT=LH/LFILE*LFIL-LM
456 IF (IT.EQ.0) GO TO 265
457 IF (TIME.GE.TIMAX) GO TO 265
458 IF (CR1(2,1).GE.CSTOP.AND.ICOND.EQ.1) GO TO 265
459 GO TO 265
460 265 CALL ABC (IMAX1,JMAX1,X,Y,LH,TIME,
461 IK,DFI,TEMP,THAX,KOT1,XO,YDIST,AMNT)
462
463 LOCATE CONTOUR POSITION AND STORE DATA
464
465 266 CONTINUE
466 CALL FRONT (IMAX1,JMAX1,LH,K,TEMP,DFI,DELT,JSTEP,0,KOT1,XDIST)
467 270 CONTINUE
468
469 GO TO NEXT TIME STEP
470
471 IF (CR1(2,1).GE.CSTOP.AND.ICOND.EQ.1) GO TO 290
472 IF (TIME.GE.TIMAX) GO TO 290
473 XO(1)=XO(2)
474 DO 280 I=2,IMAX1
475 280 XOLAST(I)=XO(I)
476 GO TO 80
477 290 IF (JSTEP.GT.1.AND.ICOND.EQ.1) GO TO 300
478 GO TO 310
479 300 TIMAX=TIME+1.

```

```

480 IF (AMRNT.NE.3) TIME=TIME+ORDTMAX
481 ICOND=2
482 GO TO 40
483 IF (LM.EQ.0) PRINT 450
484 STOP
485
C
486 320 FORMAT (A4,4A4,2F10.3)
487 330 FORMAT (1H0.20X,'IMPURITY = ',4A4,2X,'IMPURITY TYPE = ',A4)
488 340 FORMAT (1H0.20X,'... PREDEPOSITION CYCLE ...')
489 350 FORMAT (1H1.20X,'... REDISTRIBUTION CYCLE ...')
490 360 FORMAT (8I10)
491 370 FORMAT (8E10.5)
492 380 FORMAT (15A4,15,F15.9)
493 390 FORMAT (///,1H0.10X,'INI = ',D10.3,5X,'DFI = ',D10.3,/)
494 400 FORMAT (///,1H0.10X,'ITERATION DID NOT CONVERGE, ERROR = ',D10.3)
495 410 FORMAT (1H1.10X,'... SOLUTION OF DIFFUSION PROBLEM FOR SILICON,
1 ON SAPPHIRE ...//1H0.31X,'NORMALIZED SOLUTION//1H .10X,15A4//1
496 1H0.10X,'... FOLLOWING ARE THE DATA VALUES')
497 420 FORMAT (///,1H0.10X,'INI - INTRINSIC CARRIER CONC.//1H .10X,'DFI =
1 .INTRINSIC DIFFUSIVITY OF ',1X,4A4,2X,'AT ',2X,D10.3,2X,'DEG. CENT.
498 2//1H .10X,'LAMDA = LAMDA**2 = DFI*THAX/(YMAX*1.E-4**2)//1H .10X,
499 3,LAMDA = ',D10.3,5X,'FOR NORMALIZATION TIME = ',E12.6,2X,'SEC.')
500 421 FORMAT (///,1H0.10X,'AMBIENT = ',2A4/1H0.5X,'CRYSTAL ORIENTATION = ',
501 4A4//1H0.5X,'OXIDATION PARAMETERS',5X,2X,'B = ',
502 6E10.3,2X,'C = ',E10.3,/)
503 430 FORMAT (1H0.10X,'... INITIAL PROFILE AT TIME STEP = ',15,2X,'TIME
504 1= ',D10.3,2X,'HAS BEEN READ IN FROM DATA FILE 11 ...//1H0.15X,'FOI
505 2LOWING DATA ARE PROVIDED//1H .15X,'TEMP = ',D10.3,2X,'LAMDA**2 =
506 3',D10.3,2X/1H .15X,'NORM. TIME = ',D10.3,2X,'IMAX1 = ',110,2X,'JM
507 4AX1 = ',110,2X,'OXIDE GRID = ',15)
508 440 FORMAT (1H0.10X,'... FOLLOWING DATA ARE OBTAINED FROM THE DATA
509 1 . FILE 9 ...//1H .10X,'TEMP = ',F10.3/1H .10X,'LAMDA**2 = ',D10.
510 23/1H .10X,'TIME STEP = ',110/1H .10X,'IMAX1 = ',15/1H .10X,'JMAX1
511 3 = ',15)
512 450 FORMAT (1H0.10X,'...DATA INPUT ERROR ...//1H0.5X,'RUNSTREAM TERMIN
513 1ATED')
514
C
515 END
516
517
518

```

SPRT 5059.SHREJN:MAIN-PLOT

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CCC

MICRON-SnS2(1).MAIN-PLOT

•• ISOCONCENTRATION PLOT PROGRAM ••

READ IN FROM DATA DECK
FIRST CARD: LL = # OF TIME STEPS TO BE PLOTTED
SECOND CARD: IIT = TIME STEPS TO BE SKIPPED WHILE
PLOTTING PROFILE. DEFAULT PLOT AT
TIME STEPS 1 AND AT LL. FIELD 13.

```

10 DIMENSION CR(64,64),XC(64),YC(64),XO(64)
11 DATA XMAX,YMAX/8.0,4.0/OK/3.6/
12 DATA IIDL,IHLNK/IHL,IH /
13 DATA HGT/0.0875/
14 READ(5,3) LL
15 READ(5,3) IIT
16 FORMAT(13)
17 C. * READ DATA FILE 11
18 DO 100 I=1,LL
19 READ(7,4) MARK
20 FORMAT(1H0,A6)
21 IF(MARK.NE.IIDL) GO TO 5
22 READ(7,1) DFI,THAY,TEMP,YDIST
23 READ(7,2) K,IMAX,JMAX,IAMBNT
24 IK=IMAX
25 JK=JMAX
26 FORMAT(1H,5E15.9)
27 FORMAT(1H,8I10)
28 READ(7,1) (XC(I),I=2,IK)
29 READ(7,1) (YC(I),I=1,JK)
30 READ(7,4) MARK
31 S. CONTINUE
32 READ(7,2) LH
33 READ(7,1) TIME
34 DO 99 J=JK,1,-1
35 READ(7,1) (CB(I,J),I=2,IK)
36 DO 60 I=2,IK
37 IF(CB(I,J).LE.1.E-30) CB(I,J)=1.E-30
38 99 CONTINUE
39 READ(7,1) (XO(I),I=2,IK)
40 IS=L/IIT+IIT-L
41 IF(IS.EQ.0) GO TO 11
42 IF(L.EQ.1.OR.L.EQ.LL) GO TO 11
43 GO TO 100
44 11 CONTINUE
45 C. * INITIALIZE PLOT.
46 CALL PLOTS(10.0,10.0)
47 C. * RESET PEN TO ORIGIN
48 CALL PLOT(1.0,2.0,-3)
49 C. * DRAW BORDER
50 CALL PLOT(0.0,YMAX,2,-1)
51 CALL PLOT(XMAX,YMAX,2,-1)
52 CALL PLOT(XMAX,0.0,2,-1)
53 CALL PLOT(0.0,0.0,2,-1)
54 C. * DRAW OXIDE MASK
55 XP=(XC(IK)-2.)
56 IF(IAMBNT.NE.3) XP=(XC(IK)-2.E-4)/1.E-4
57 OX=(A./XP)*XC(IK)
58 CALL PLOT(OX,YMAX,3)
59 CALL PLOT(OX,YMAX,0.2,2,-1)
60 CALL PLOT(XMAX,YMAX,0.2,2,-1)
61 CALL PLOT(XMAX,YMAX,2,-1)
62 X=XMAX
63 PAY=8.-OX
64 INC=INT(PAY/0.2)
65 DO 10 I=1,INC
66 X=X-0.2
67 CALL PLOT(X,YMAX,0.2,2,-1)
68 CALL PLOT(X,YMAX,3)
69 10 CONTINUE
70 CALL PLOT(0.0,0.0,3)
71 C. * HORIZONTAL GRID LINES
72 DO 20 I=1,9
73 Y=0.4*FLOAT(I)
74 LNWT=3
75 IF(I.EQ.5) LNWT=1
76 CALL PLOT(0.0,Y,3)
77 CALL PLOT(XMAX,Y,2,LNWT)
78 20 CONTINUE
79 C. * VERTICAL GRID LINES

```

```

80 DO 30 I=1,17
81 X=0.4*FLOAT(I)
82 LNWT=3
83 IF (MOD(I,5).EQ.0) LNWT=1
84 CALL PLOT(X,0.0,3)
85 CALL PLOT(X,YMAX,2,LNWT)
86
87 30 CONTINUE
88 * HORIZONTAL AXIS NUMBERS
89 DEY=XP/20.
90 IE=21
91 IS=1
92 IF (DEX.LY.0.1) IE=11
93 IF (DEX.LY.0.1) IS=2
94 IF (DEX.LY.0.01) DEY=XP/10.
95 IF (IAMBNT.EQ.3) GO TO 31
96 IS=1
97 DEY=XP/20.
98 IE=21
99
100 31 CONTINUE
101 DO 40 I=1,12
102 VAL=DEX*FLOAT(I-1)
103 X=0.4*FLOAT(I-1)-1.5*HGT+0.04
104 Y=0.2
105 CALL NUMBER(X,Y,HGT,VAL,0.0,16)
106
107 40 CONTINUE
108 * VERTICAL AXIS NUMBERS
109 IF (IAMBNT.NE.3) YAK=YC(JK)/1.E-4
110 DEY=YAK/10.
111 DO 50 I=1,11
112 VAL=DEY*FLOAT(I-1)
113 X=-3.0*HGT-0.1
114 Y=VMAX-0.4*FLOAT(I-1)-0.5*HGT
115 CALL NUMBER(X,Y,HGT,VAL,0.0,1)
116
117 50 CONTINUE
118 CALL SYMBOL(4.2,5.7,0.1,1,1.0E20,0.0,0.8)
119 CALL SYMBOL(4.2,5.5,0.1,1,1.0E19,0.0,0.8)
120 CALL SYMBOL(4.2,5.3,0.1,1,1.0E18,0.0,0.8)
121 CALL SYMBOL(4.2,5.1,0.1,1,1.0E17,0.0,0.8)
122 CALL SYMBOL(4.2,4.9,0.1,1,1.0E16,0.0,0.8)
123 CALL SYMBOL(4.2,4.7,0.1,1,1.0E15,0.0,0.8)
124 CALL SYMBOL(4.0,5.7,0.1,0,0.0,0.1)
125 CALL SYMBOL(4.0,5.5,0.1,0,0.0,0.1)
126 CALL SYMBOL(4.0,5.3,0.1,0,0.0,0.1)
127 CALL SYMBOL(4.0,5.1,0.1,0,0.0,0.1)
128 CALL SYMBOL(4.0,4.9,0.1,0,0.0,0.1)
129 CALL SYMBOL(4.0,4.7,0.1,0,0.0,0.1)
130 CALL SYMBOL(0.0,5.4,0.2,1,0.0,0.1) = '0.0,14)
131 CALL SYMBOL(0.0,5.4,0.2,1,0.0,0.1)
132 CALL NUMBER(2.6,5.4,0.2,0,1,0.0,4)
133 CALL SYMBOL(0.0,5.1,0.2,TEMPERATURE = '0.0,14)
134 CALL NUMBER(2.6,5.1,0.2,TEMP,0.0,0)
135 CALL SYMBOL(0.0,4.8,0.2,TIME STP = '0.0,14)
136 TLM=LM
137 CALL NUMBER(2.6,4.8,0.2,TLH,0.0,0.1)
138 CALL SYMBOL(0.0,4.5,0.2,TIME = '0.0,14)
139 CALL NUMBER(2.6,4.5,0.2,TIME,0.0,0.2)
140 DO 200 II=1,6
141 CONVAL=10.0*FLOAT(20-II+1)
142 CALL PLTCONICB,CONVAL,II,IK,JK)
143
144 200 CONTINUE
145 CALL PLOT(0.0,0.0,999)
146 100 CONTINUE
147 STOP
148 END

```

8FIN

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APPENDIX D.

FINITE-ELEMENT EVALUATION

In order to better understand the applicability of the finite element method, it was applied to a one-dimensional linear diffusion problem. This simple problem is one for which familiar results are available for comparison and at the same time taxes the finite-element method. In its most valid form, the finite element method is applicable to variational problems in which a true minimum of an energy-related function exists. Such a minimum does not apply for the semiconductor problem in which current flow occurs by diffusive and conductive mechanisms. It has been proposed that a "weak form", the so-called Galerkin method, be applied to such problems. The typical semiconductor problem is a non-linear boundary value and initial condition problem of which the linear diffusion problem is a very special case. In the example chosen, the diffusion variable u , obeys:

$$u(x,t)|_{x=0} = u_s = 1 \quad (a) \quad (D.1)$$

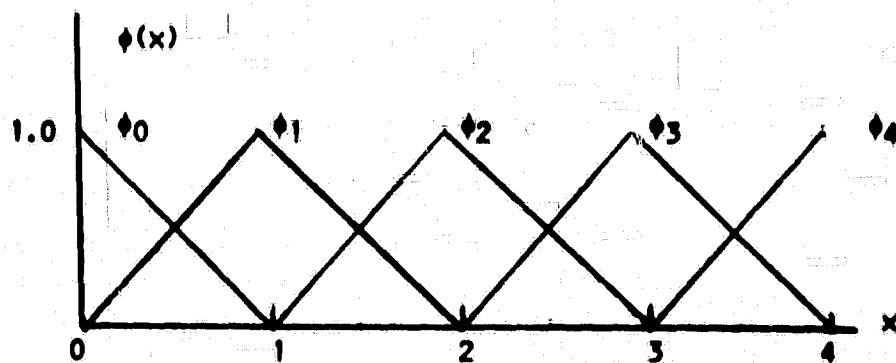
$$u_x(x,t)|_{x=a} = 0 \quad (b)$$

$$u(x,t)|_{t=0} = \begin{matrix} 1, & x=0 \\ 0, & x>0 \end{matrix} \quad (c)$$

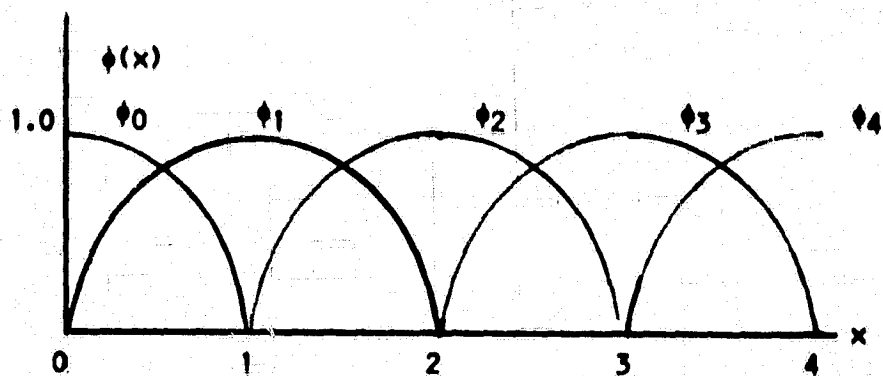
$$u_t - u_{xx} = f(x,t) = 0 \quad (D.2)$$

The Galerkin formulation of this problem is:

$$\int_0^a (u_t v - u_x v_x - f v) dx = 0 \quad (D.3)$$



(a) Bilinear hill functions



(b) Bicubic (Hermite) hill functions

Figure D-1. Illustration of hill functions used in finite element method.

where $v(x,t)$ represents a "trial function" which is used to approximate $u(x,t)$. The finite element method uses a set of "hill functions" as illustrated in Figure D.1 to construct the $v(x,t)$ approximation. Two of the popular hill functions are the Hermite bicubic and the bilinear functions which are illustrated in the figure and were used in the example. The final form of the approximate solution is;

$$v(x,t) = \sum_{i=1}^N q_i(t) \phi_i(x) \quad (D.4)$$

On the node points the solution is approximated by the set $\{q_i(t)\}$ for the type of hill functions which overlap as illustrated in Figure D-1. Solution for the set $\{q_i(t)\}$ is then analogous to solving for the set $\{u_i(t)\}$ on the node points using the finite difference technique. The equations for the set $\{q_i(t)\}$ are obtained by substituting (D-4) into (D-3).

$$\sum_{i=1}^N \int_0^a \left(\frac{\partial q_i}{\partial t} \phi_i \phi_j + q_i \frac{\partial \phi_i}{\partial x} \frac{\partial \phi_j}{\partial x} + f \phi_j \right) dx = 0$$

$$j = 1, 2, 3, \dots, N \quad (D.5)$$

From (D-5) a set of time differential equations is obtained which is solved using an implicit numerical method.

The solution of the problem posed by the example is closely approximated by the erfc function in the range $0 \leq x \leq 3$ if $a=6$, and this solution was used to compare the accuracy of the finite element and finite difference methods. Figures D-2, D-4 show the

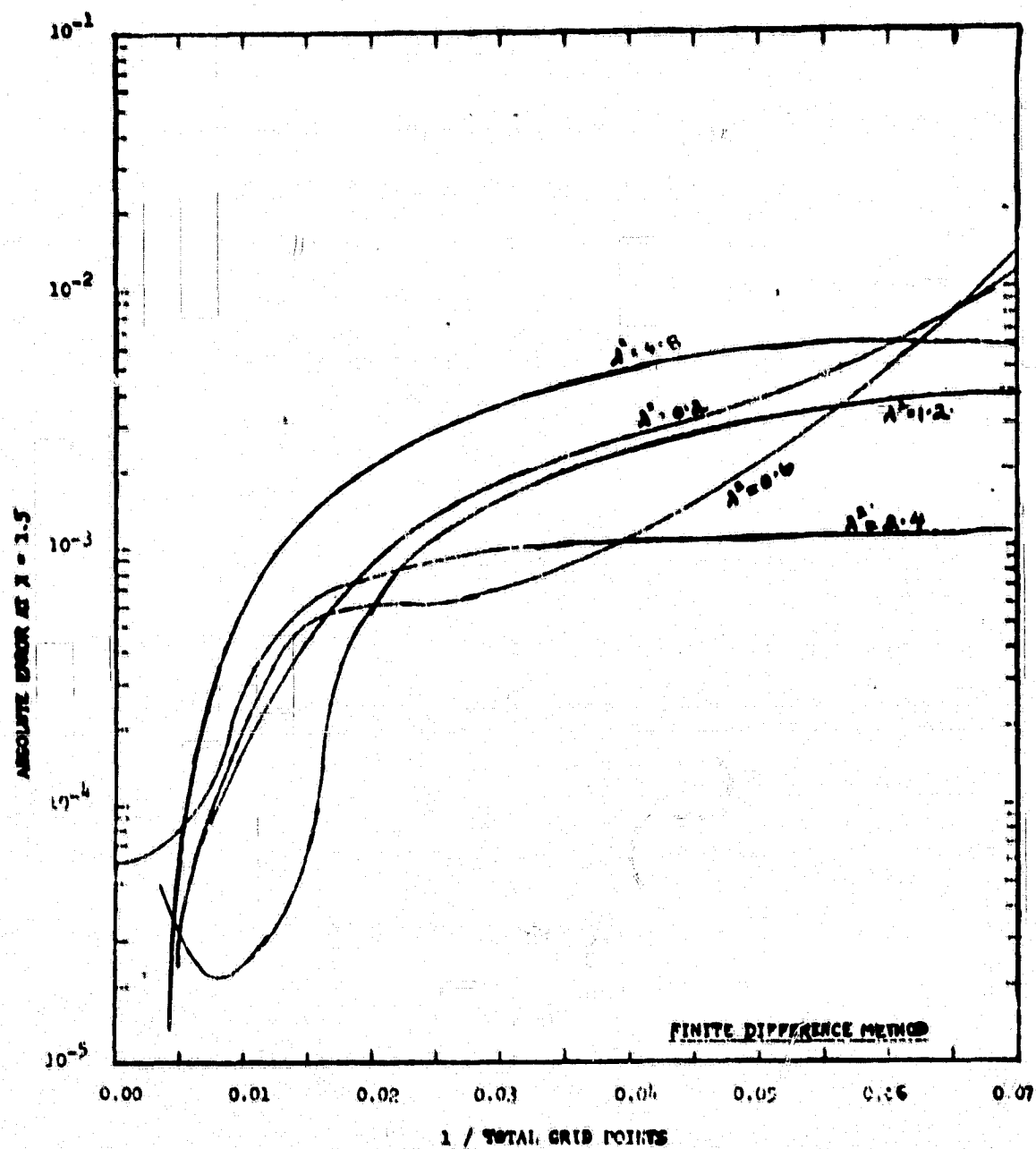


Figure D-2. Error for finite-difference vs, reciprocal of total number of grid points.

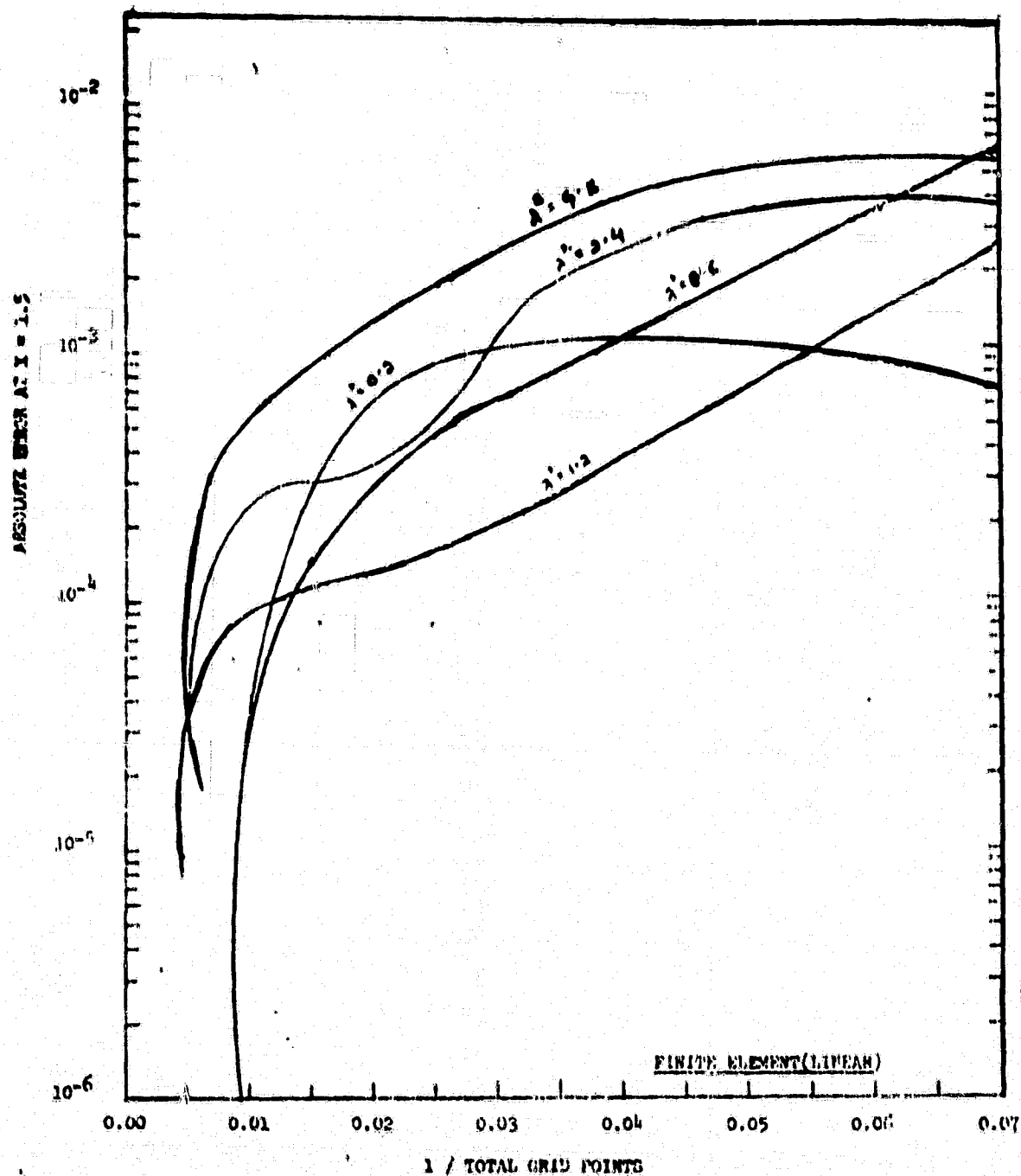


Figure D-3. Error for finite-bilinear element vs. reciprocal of total number of grid points.

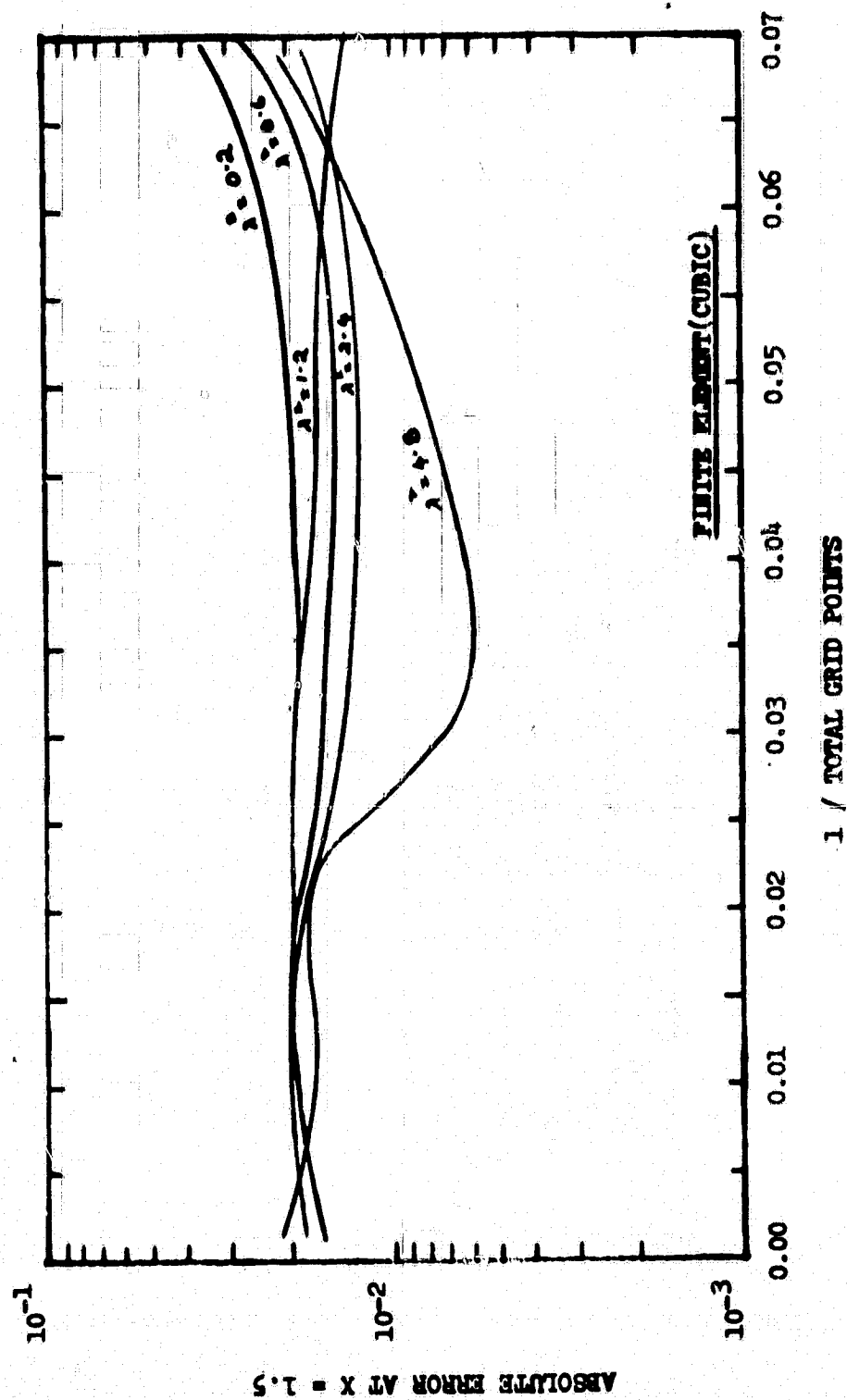


Figure D-4. Error for finite-bicubic-element vs. reciprocal of total number of grid points.

maximum error as a function of the reciprocal of the number of grid points and the size of the time step, i.e. $\lambda^2 = \Delta t / \Delta x^2$.

The error obtained in the solution by the bilinear finite element method is very nearly the same as that obtained with the finite difference method. This was not surprising because the system of equations for $\{q_1(t)\}$ and $\{u_1(t)\}$ were quite similar. What was surprising was that the Hermite bicubic finite element produced such poor results, although this surprise was based upon the intuition that since this element was more difficult to use it should provide some reward for the difficulty.

APPENDIX E

MICROELECTRONICS AT MISSISSIPPI STATE UNIVERSITY

A. Introduction

The new microelectronics facility at Mississippi State consists of approximately 6600 square feet of space located in the newly constructed (1977) Harry Charles Fleming Simrall Electrical Engineering Building. The space and equipment represent a million dollars investment. Approximately 3000 square feet consists of class 10,000 clean rooms. Within this space, facilities exist for mask-making and photolithography, for chemical preparation, oxidation, etching, diffusion of impurities, for metallization, die-bonding and lead attachment, and for the evaluation of device and integrated circuit parameters. In addition, the hybrid facilities allows fabrication of thick and thin film circuits and encapsulation. Close research ties with NASA Marshall Space Flight Center makes available to EE students and faculty additional research tools, including scanning electron microscope, Auger analysis, electron microprobe, etc.

The vast field of solid state electronics has experienced radical changes since the invention of the transistor in 1949, and the invention of the integrated circuit in 1959. Today's hand held calculator, for instance, contains more than 50,000 active solid

state devices on a single substrate (called a "chip"); electronic watches and appliances touch every aspect of our daily lives.

The rapidly changing technology which has made such electronic marvels possible poses a continuing challenge to an electrical engineering faculty not only to keep abreast, but to devise a curriculum which passes such knowledge on to students, both graduate and undergraduate, and to motivate them in a manner adequate to enable them to join that technology as actively contributing graduate engineers. To this end, the Electrical Engineering Department at Mississippi State University has recently established an extensive laboratory facility and revised curriculum aimed at meeting the threefold purpose of transmitting knowledge through teaching, at the undergraduate and graduate levels; opening new frontiers through research; and extending these efforts and findings to others through service.

Success in these endeavors depends on several important ingredients:

- 1) A dedicated faculty possessing interest and expertise in the various areas of physical electronics.
- 2) An undergraduate curriculum devised to teach students not only fundamental principles of physical electronics and of solid state electron devices, but also of the technology which is used in their realization. Students should be provided the opportunity to achieve "hands-on" experience in device fabrication.
- 3) A graduate teaching program offering education which enables students to do practical design and creative research contributing to the state-of-the-art.

4) A comprehensive research program which simultaneously provides for the education of advanced students while contributing knowledge, basic and applied, to the advancement of the field.

5) The availability of adequate laboratory facilities to support both teaching and research activities.

B. New Electrical Engineering Facilities

The Harry Charles F. Simrall Electrical Engineering building was completed in January, 1977, consisting of 95,000 square feet of floor space at a construction cost of 4.25 million dollars. This building was built under the direction of the State of Mississippi Building Commission with funds appropriated by the State Legislature.

The general theme of the building is classrooms, computer terminal and other heavily populated areas on the first floor, department offices and student activity areas on the second floor with teaching and research laboratories on the third and fourth floors. The features of the Harry Charles F. Simrall Electrical Engineering building include:

- 1) 10 classrooms with 382 seats total.
- 2) Computer terminal operated by computing center housing 1004 terminal and other special purpose equipment.
- 3) 254 seat Auditorium.
- 4) Microelectronics laboratory complex for instruction and research.
- 5) High voltage laboratory complex for instruction and research and testing.

6) Computer design and application laboratory complex for instruction and research.

7) Dedicated laboratories for instruction and research in control systems, microwave systems, communication systems, and electronic systems.

8) Dedicated instructional laboratories for study of digital devices, networks and electronics.

9) Student activities and organization area.

10) Faculty and Departmental office complex.

The building now houses all programs and activities of the Electrical Engineering Department which have previously been housed in parts of five buildings.

The Electrical Engineering Department includes 26 faculty members, some with duties outside the department, 410 undergraduate electrical engineering students, 42 undergraduate electronic engineering technology students and some 45 electrical engineering graduate students for a total enrollment of some 500 students.

C. Microelectronics

The objectives of the microelectronics program at Mississippi State are consistent with the University charge to provide education, research and service. These objectives are:

1) To provide an outstanding facility for research dealing with the electronic properties of materials, electron device research, circuit fabrication technology, and computer aided design of electronic circuits.

2) To provide circuit technology accessible at several levels of sophistication which will support research and teaching activities within the department, college and University.

3) To provide a facility available for prototype development of electronic apparatus by industrial concerns and to provide an expertise in electronic fabrication technology to assist industrial start-up operations.

4) To provide operational strategies to allow utilization of the facilities on an economically feasible basis consistent with the commitment to supporting agencies.

The SCOPE of the developing facility is detailed below:

I. Fabrication and processing capability

A. Silicon Integrated Circuit

1. Thermal oxidation and impurity diffusion
2. Photolithography
3. Chemical vapor deposition
 - a. Polysilicon
 - b. silicon dioxide
 - c. other (phosphosilicate glass, silicon nitride, etc.)
4. Aluminum film deposition
 - a. sputtering
 - b. E-beam evaporation
5. Epitaxial silicon
6. Ion-implantation

B. Hybrid Integrated Circuits

1. Thick film screen printing and firing

2. Chip and wire bonding
3. Component trimming
4. Substrate scribing
5. Packaging and encapsulation

C. Printed Circuits

1. Board sensitization, exposure, and development
2. Board etching and drilling
3. Board plating
4. Board lamination

II. Computer Aided Design

A. Art work generation by computer

1. Printed circuit layout from line drawing
2. Custom art work for hybrid and monolithic IC's
3. Art work from cell libraries and layout programs

B. Art work processing

1. Reduction
2. Step and repeat reduction of IC master masks

(presently thru NASA)

3. Development of working masks

C. Circuit Analysis

1. PCAP
2. Nonlinear circuit analysis program
3. Digital logic and timing analysis

III. Experimental Evaluation

- #### A. Electrical: C-V, sheet resistance, curve tracing, probe testing, circuit testing.

- B. Electrochemical: lap and stain, anodization
- C. Optical: Microscopic, interferometric, ellipsometric
- D. Surface analysis: SEM with SIMS or Auger attachment
(presently thru NASA)

D. Description of Facilities

As indicated earlier, the new \$4.25 million Harry F. C. Simrall Electrical Engineering Building became occupied in January of 1977. In the electronics area, the department owned or had custody of approximately \$250,000 worth of equipment related to microelectronics prior to moving into the new facilities. Primarily the existing equipment consisted of that furnished by the state (mostly in the in the past 3 to 5 years), surplus equipment from NASA, much built in-house, and GFE items.

The microelectronics facilities are located on the fourth floor of the building and consume in excess of 6,600 square feet. Approximately 3,000 square feet of this consist of class 10,000 clean rooms. At a conservative building cost of \$45 per square foot, this represents approximately a \$300,000 investment in floor space alone. In addition, the department either has purchased or is in the process of purchasing some \$175,000 worth of new equipment to furnish the microelectronics laboratory and associated supporting labs. Thus, a total commitment by the University of well over a half million dollars is being invested in this area for purposes of fundamental research and teaching. In addition, equipment obtained through industrial donations represents well over \$350,000 to date.

Through University acquisition and industrial donations, the department will be equipped to do significant research in silicon integrated circuits, thick film and chip hybrid circuits.

The following describes the fourth floor microelectronics laboratories and related support facilities. All rooms have compressed air, vacuum, chemical drains, and extensive venting for safe and convenient operation.

A. Silicon Fabrication

This activity is to be carried out in three different rooms, all class 10,000. The water supply consists of an evaporation still, a storage tank with ultraviolet light source, a deionizer, and submicron filters for delivering a minimum of two gallon/minute of 15-18 megohm/cm. water.

A1. Process Room

This large 30 x 40 foot room has one fume hood with etching sink and D. I. water. Benches and cabinets and a quartz/mullite tube closet are also included. There exist five vented gas bottle closets capable of storing ten large cylinders. Water, drains and 3-phase power are available for furnaces and reactor equipment. The basic equipment includes:

- . Thermco Spartan 6-tube furnace with class-100 load station and source cabinets.
- . Three single tube furnaces (Lindberg, Marshall and BTU), all with electronic controls.
- . One class 100 clean bench

- . Vaponics deionized water system with additional reservoir for continuous cycle filtering
- . Wafer dicer
- . Unicorp. Inc. Unipole VIII Epitaxial reactor with dual 8" susceptors driven by a LEPEL solid state power supply (143KVA)
- . Four point probe
- . Lap and stain facilities
- . Ellipsometer/Laser source
- . Microscopes
- . Multiple probe station
- . Capacitance-Voltage test station
- . Anodization equipment
- . Large dewars for liquid nitrogen and liquid oxygen

For the furnaces, two tubes will be equipped to operate as hot-walled low pressure CVD reactors. The remaining tubes will be used for diffusion and oxidation. One or more tubes will be available for non-silicon work.

A2. Photolithographic Room

This room is 10 x 24 feet and is equipped with three in-line class 100 clean benches and two pass-through ovens with nitrogen ambients. All photo resist and developing operations are done in class 100 environment. Photo-resist spinning is done under temperature and humidity control. Oxide etching and wafer washing is done in end stations with high quality water. Other equipment includes:

- . Two-head spinner, plus a single-head spinner

. Electroglass mask aligner for 1 1/2" wafers, plus two Casper aligners for 1 1/2" to 3" wafers

- . Balance table's
- . Interference microscope
- . Hot plate/stirrers, etc.

A3. Metallization and Bonding Room

This large 30 x 20 foot class 10,000 clean room is for the deposition of metal films and thermal-compression bonding. It is equipped with compressed air, vacuum, D. I. water and chemical drains. Pertinent equipment includes:

- . NRC-Varian 6" diffusion pump vacuum station equipped with a Sloan sputtering system and a thickness monitor
- . Hughes pulse tip thermal compression bonder
- . Class 100 clean station for bonder
- . Varion Vacion vacuum station equipped for thermal evaporation of aluminum including film thickness monitor and class 100 clean station
- . Class 100 clean benches for multiple probe station and vacuum system work areas
- . Work benches and cabinets
- . Large dewars for liquid nitrogen
- . A 200 KeV ion implanter is to be added to this room in early 1979.
- . Perkin-Elmer Vacion vacuum station equipped with dual E-beam guns for depositing alloys.

B. Hybrid Fabrication

This activity will be carried out in one large 48 x 42 foot room equipped with fume heads, sinks compressed air, vacuum and three-phase power. Ample bench tops and storage cabinet space is also available. Equipment includes:

- . Thick film screen printer
- . Class 100 clean bench for printer
- . Drying oven
- . Thermco belt furnace
- . Thick film trimmer
- . Thick film trimmer
- . Multiple probe station
- . Electronic instrumentation for circuit evaluation
- . Packaging and sealing station

C. Artwork and Mask Making

This work will be carried out in four different rooms.

C1. Computer Aided Plotting Room

This 30 x 50 foot room was initially scheduled for all artwork but a more comprehensive computer aided graphics facility is being developed. Equipment includes:

- . Gerber Scientific 1200 plotter with HP minicomputer tape drive (36 x 36 inch plotting surface with ink or photo exposure heads)
- . Tektronix graphics terminal with hard copy capability
- . Uniscope CRT terminal to the central campus UNIVAC 1108 computer

- . Data General Eclipse S/130 minicomputer with video monitors and Varian Statos 42 high density electrostatic printer/plotter

- . Lexidata color graphics terminal

- . Digitizing table for generating check plots on Gerber plotter

C2. Manual Graphics

This will be done in the reduction room. Equipment includes drafting tables and a Unitech coordinatograph with digital read-out. Ruby lith masks are produced with this system.

C3. Dark Room

This is a small dark room with modern developing sink temperature controlled water source, and ample storage cabinets and bench top space.

C4. Reduction Room

This room is part of the printed circuits lab and is equipped with a precision Dekacon reduction camera (36 x 36 inch mask mounting capabilities).

C5. Step and Repeat Room

This is an 8 x 24 foot class 10,000 clean room and is part of the silicon IC complex. It is equipped with two class 100 clean benches. One bench has a sink and hood for development and one bench is for a step and repeat camera. The first bench is equipped with compressed air, nitrogen blow gun, and a DI submicron filtered water.

It is hoped that a step and repeat camera will be added soon.

D. Printed Circuit Lab

This laboratory is equipped with benches, a fume hood and sink, and two spray etchers, water dryer, KPR developer unit, IR oven, dip coater, rinse unit, shear, pilot hole punch, drill press, light table, etc. Almost all of this equipment is new.

E. Other Equipment

The microelectronics laboratory has a wide assortment of electronic equipment for evaluation of semiconductor devices and circuits, including signal sources, meters, counters, curve tracers, scopes, etc. A partial listing of new equipment just purchased includes:

- . 100 meg Hz Oscilloscope (Tektronics Mod 465);
- . Sampling Oscilloscope (HP Mod 182C main frame with HP 1810A sampler);
- . Digital to Analog Converter, HP 49303A;
- . X-Y recorder, HP Mod. 7015;
- . LRC meter, HP Mod 4332A;
- . Precision multimeters, HP 3490A;
- . Interface bus, HP 59310A;
- . etc.

F. Supporting Laboratories

F1. Electro-optic Laboratory

This lab is equipped with a vibration free table, optical benches, detectors, lens, filter, optical radiation detector, two lasers (5 watt argon and 100 milliwatt Helium-Neon), and several items of standard electronic instrumentation.

F2. Communications Laboratory

This facility includes extensive electronic instrumentation for microwave measurements and for signal analysis. Equipment includes wave guides, slotted lines, microwave sources, UHF sources, wave analyzers, antennas, etc. New equipment will include a spectrum analyzer (up to 1.8 G Hz) and a vector voltmeter for s-parameter measurements. Also included are maximal length pseudo-random noise generators and bit pattern generators. The laboratory is located in two rooms on the fourth floor and has two antenna locations on the roof of the building.

F3. Instruction Laboratory

Two large rooms and several smaller rooms are dedicated to teaching and project laboratories. A wide variety of instrumentation, breadboarding equipment, logic trainers, power supplies, etc. are available for instruction, training and project work.

APPENDIX F

POST-HEAT TREATMENT EFFECTS ON DOUBLE LAYER METAL STRUCTURES FOR VLSI APPLICATIONS

A. Introduction

The increasing demands toward greater packing densities in LSI and VLSI make it imperative that multilevel metallization systems be developed. Although several reviews have been written [F1-7], the realization of reproducible and reliable results have yet to be forthcoming. The most common problem associated with double layer metal has been the inability to make electrical contacts between metal layers through via holes etched in the dielectric to provide electrical communication between metals. The problem is more acute when the number of vias is large (>500) and are relatively small in size (≤ 0.2 mil square). Another, less important problem is associated with shorts between metal layers due to pinholes in the dielectric film, thin spots, or poor coverage of hillocks in the first level metal. An example of the use of double layer metal for circuit application [F-8] is given in Figure F-1.

In order to study the effects associated with double layer metal structures having a large number of small vias, a test pattern was generated consisting of a string of 560 vias. The via size was varied from 0.5 mil square to 0.2 mil square per string. Electrical measurements were made on the test pattern after initial sintering and subsequent heat treatments in order to monitor

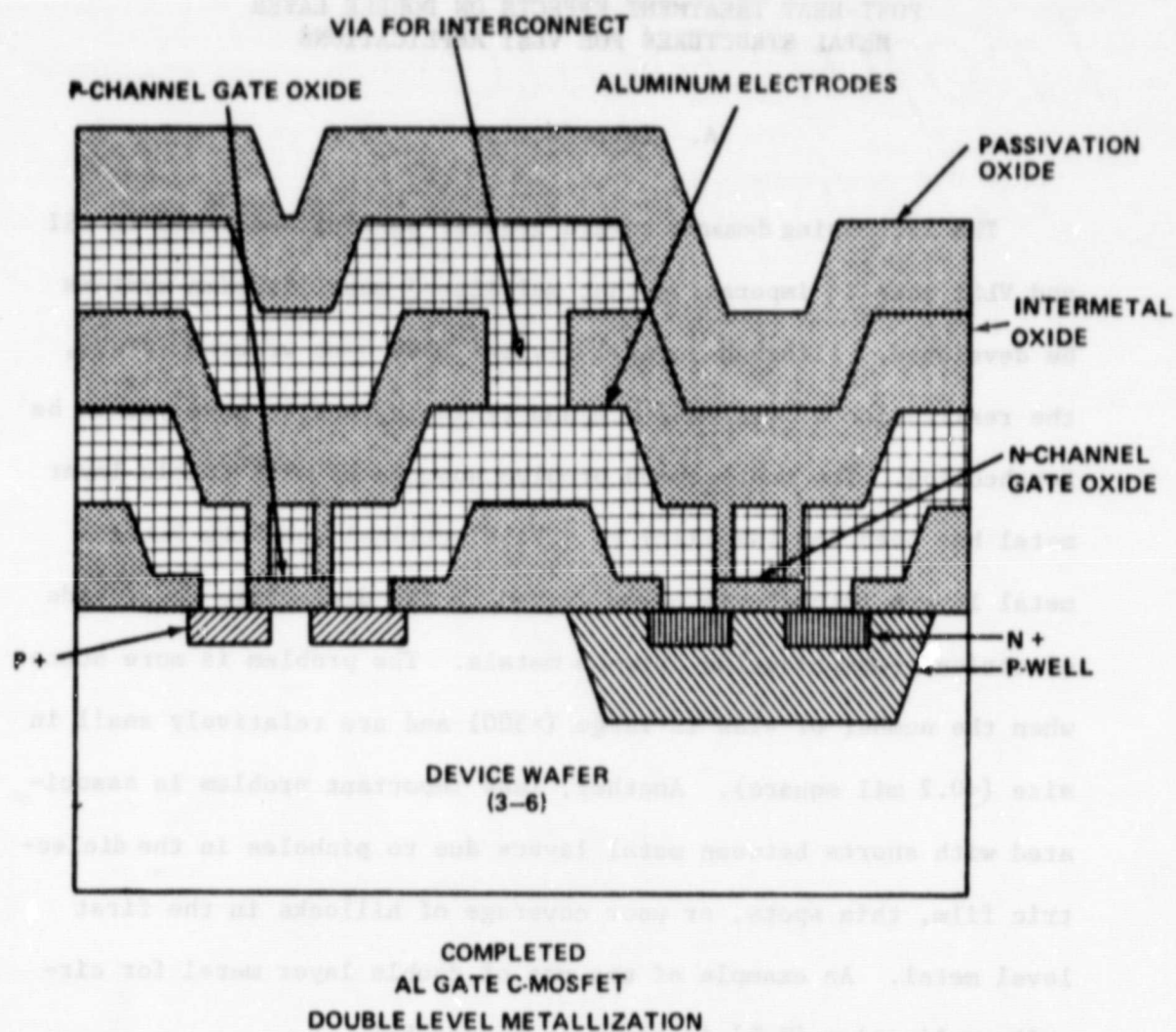


Figure F-1. An example of the use of double layer metal in the realization of an aluminum gate C-MOSFET structure.

contact resistance behavior and variations in yield. Metal interconnects between vias were typically 0.7 mils wide although samples were also prepared and tested having interconnects of 0.4, 0.5, and 0.6 mil wide Al, with little or no variation in results.

B. Preparation of Test Vehicle

The steps involved in preparing the test vehicle consist of the following. The starting material was 3-8 ohm-cm, (100) oriented, n-type phosphorous doped silicon wafers. A field oxide was thermally grown in dry O_2 for 5 minutes, boiling H_2O for 60 minutes and then dry O_2 for an additional 15 minutes at $900^\circ C$ resulting in an oxide thickness of $14 K^\circ A$. Prior to depositing the first layer metal, a cleaning step was performed, this consisted of a one-minute rinse in deionized water. The wafer was then dehydrated at $900^\circ C$ in an N_2 ambient for 10 minutes. The first metal layer was d.c. sputtered structural grade Al alloy 6061 of $0.5\mu m$ thickness. The metal was patterned using conventional photolithographic techniques with Waycoat-31 negative photoresist.

Prior to depositing the dielectric, scribe lines (0.7 mils wide) were etched around the test patterns through the thermally grown field oxide down to the silicon substrate. These lines were used as an etch end-point monitor in etching vias in the intermetal dielectric.

The intermetal oxide was next deposited at $400^\circ C$ using CVD of SiH_4 (4% in Ar) and O_2 (and later P_2O_5 of approximately 3 mole

percent) to a thickness of $8\text{K}^\circ\text{A}$. Dielectric thickness was measured with an (laser) ellipsometer. Vias were etched in this dielectric film with buffered HF using standard photolithographic masking. This etching was done first by dipping the wafers in a stirred solution of etchant, using the scribe lines as reference to determine when etching was completely through the dielectric film. In later processes, this etching was done ultrasonically in a totally enclosed container.

The second layer metal was also deposited using dc sputtering of the same target used in the first layer metal and patterned. Typically a 15 minute aluminum sintering process at 470°C preceded the first testing of the completed test vehicle.

C. Experimental Results

Approximately 50 wafers were processed. Each wafer had 200-220 test patterns with via sizes ranging from 0.2 mils square to 0.5 mils square. Table I represents a summary of results in terms of percent yield obtained for each via size as a function of fabrication process. Process A through L are explained below. Among other variables it will be noted that each process is characterized by an etch time associated with etching the vias in the intermetal dielectric film. The scribe lines were used as reference. When all dielectric was etched from these scribe lines, this was defined as the 'break' time. Any additional etching beyond this break time is measured in seconds.

Percentage Yield Via Resistance for 560 Vias < 20 Meg Ohm Process Identification												
Via Size	A	B	C	D	E	F	G	H	I	J	K	L
0.5 mils	81	76	95	98	99	98	94	84	94	98	98	98
0.4 mils	70	56	88	94	97	98	92	82	89	90	97	97
0.3 mils	61	53	64	85	93	94	92	83	87	80	100	100
0.2 mils	40	18	64	82	91	94	93	89	72	67	98	98

Table I-A

Percentage Yield Via Resistance for 560 Vias < 10 Kil Ohms Process Identification												
Via Size	A	B	C	D	E	F	G	H	I	J	K	L
0.5 mils	17	59	86	97	97	94	84	61	92	93	98	98
0.4 mils	8	48	73	89	94	96	88	64	82	90	97	97
0.3 mils	0	30	45	64	89	92	88	74	85	80	100	100
0.2 mils	0	14	13	26	44	59	64	52	38	67	98	98

Table I-B

Percentage Yield Via Resistance for 560 Vias < 1 Kil Ohm Process Identification												
Via Size	A	B	C	D	E	F	G	H	I	J	K	L
0.5 mils	0	59	78	85	86	82	74	56	92	92	98	98
0.4 mils	0	46	47	66	72	72	68	54	82	90	97	97
0.3 mils	0	28	85	36	47	55	58	56	85	80	100	100
0.2 mils	0	8	10	15	22	27	30	30	32	67	75	98

Table I-C

Table I Percentage yield as a function of processing with via size as a parameter for contact resistance of 560 vias less than 20 Megohm, 10 Kilohm, and 1 Kilohm for tables I-A, I-B, and I-C, respectively.

Process Definitions:

1) Wafers were processed as described in section B. The width of the first level metal interconnect of 0.4, 0.5, 0.6 and 0.7 mils corresponded to test patterns having square vias of 0.2, 0.3, 0.4, and 0.5 mils, respectively. The width of the second metal was 0.7 mils. Via etch time was break plus 10 seconds.

2) Wafers were processed as described in section B. The metal interconnects on both levels were 0.7 mils wide. (This is true for all processes 2 through 7). Via etch time was break plus 10 seconds.

3) Wafers processed as described in section B with via etch time in stirred dielectric etchant extended 20 seconds beyond break time.

4 thru 7) correspond to wafers processed as described in section B but with via etch time in stirred dielectric etchant extended 40, 60, 80, 100 and 120 seconds beyond break, respectively. (Note that the values given for processes 1) through 7) represent an average of five different process runs of eight wafers for each run.)

8) Wafers processed as described in section B but having a phosphorous doped intermetal dielectric of 3.1 mole percent (as determined by Auger spectroscopy) and with vias etched in stirred dielectric etchant for 20 seconds beyond break.

9) Wafers processed as described in 8 above except via etching was done ultrasonically in a closed container for 20 seconds beyond break.

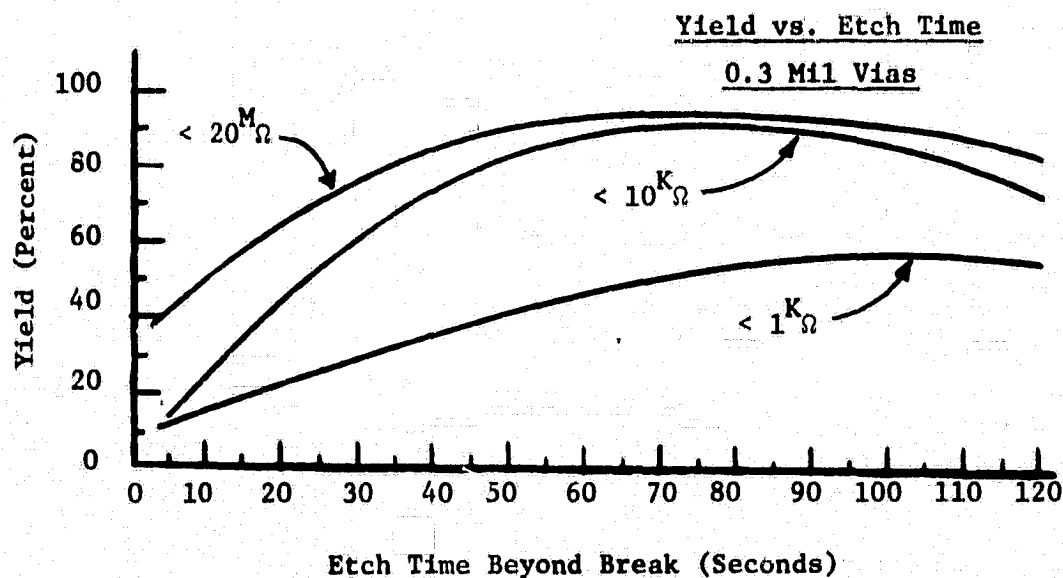
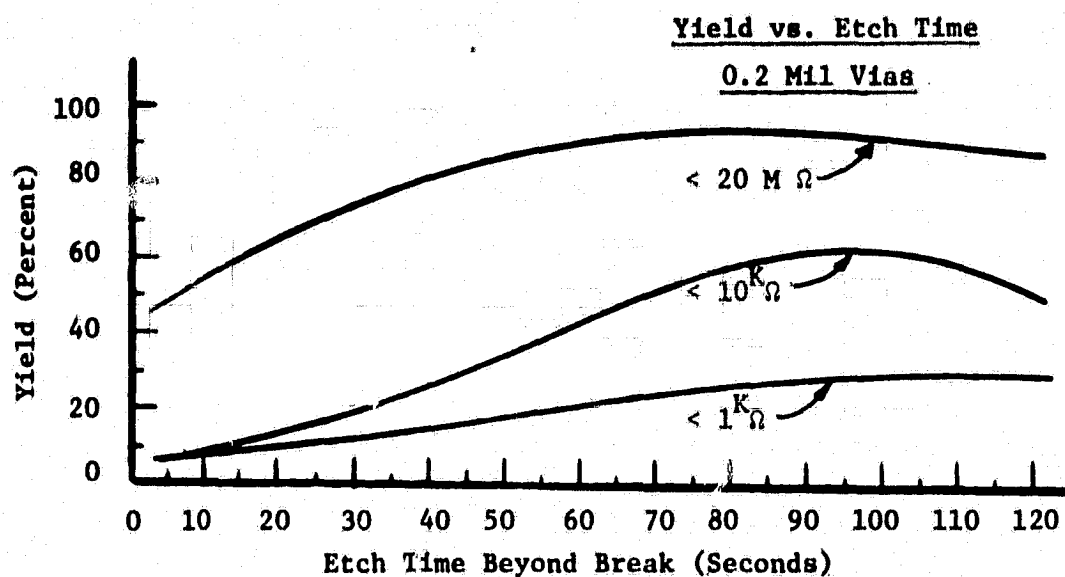


Figure F-2. Percent yield as a function of etch time beyond break with via size as a parameter. Intermetal dielectric etch accomplished with stirred B.O.E.

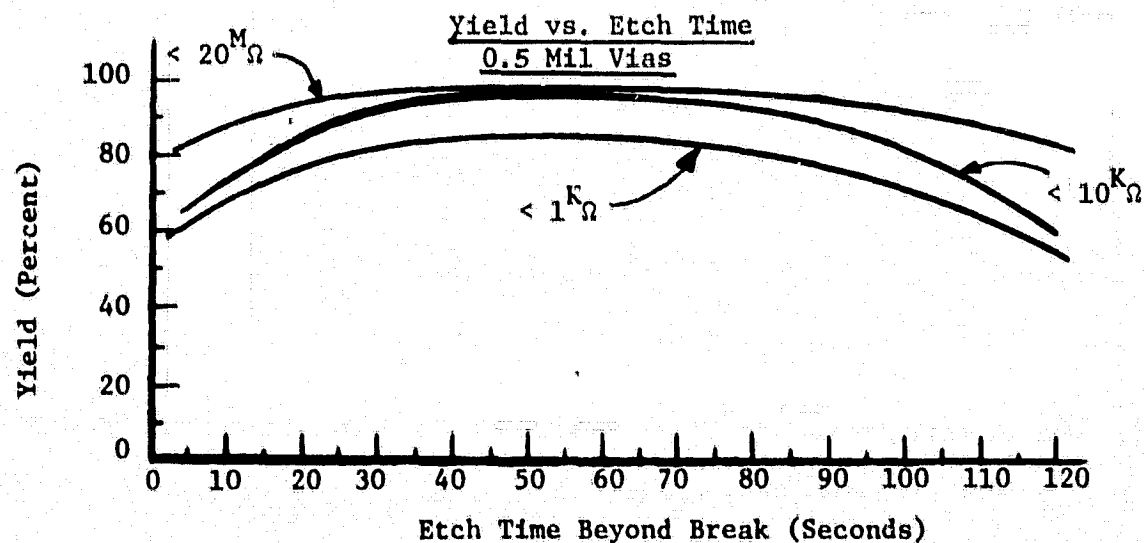
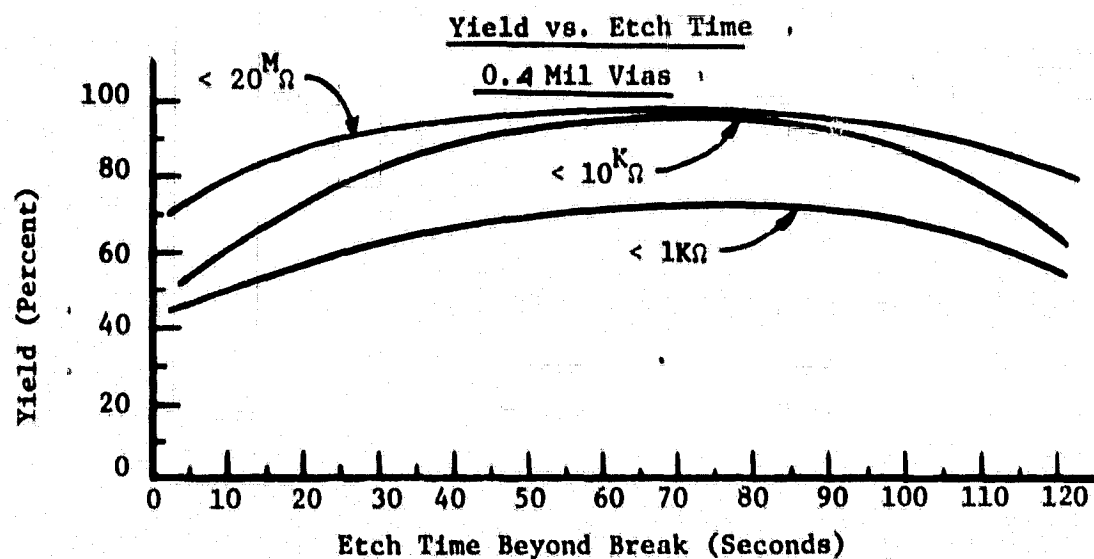


Figure F-2. (continued). Percent yield as a function of etch time beyond break with via size as a parameter. Intermetal dielectric etch accomplished with stirred B. O. E.

10) Wafers processed as described in 9 above with the addition of a first level metal cleaning step through the vias prior to depositing the second level metal. The metal cleaning solution consisted of an ethylene glycol-buffered HF-H₂O solution for the removal of Al₂O₃ from the first level metal prior to deposition of second level metal [F-10].

11) Wafers processed as described in 10 above but having undergone a one-half hour post heat (sintering) treatment at 490°C.

The results of processes 3 through 8 are displayed graphically in Figure F-2. The data are shown in Tables F1-A, B, and C which give the percent yield for via contact resistances less than 20 meg-ohms, 10 kil-ohms and 1 kil-ohm. It is desirable to have minimum contact resistance (i.e. less than 250 ohms) since as the number of vias increase from 600 to approximately 3000 for a VLSI circuit, the resistance will increase proportionately. Any pattern having a contact resistance greater than 20 meg-ohm is assumed to be an open-circuit in Table F1.

Wafers processed as described in D in Table F1 were used for an Auger surface analysis of the first level metal through a 0.5 mil via just prior to depositing the second level metal. The purpose of the Auger analysis was to determine what insulating materials reside on the surface of the first level metal which prevented good low resistance ohmic contact between metal levels. The results of this analysis indicated the following materials were present with an accuracy of $\pm 5\%$:

Al ₂ O ₃	64%
C	31%
N	1.8%
Mg	1.3%
Si	0.6%
F	0.6%
S	0.7%
O (other than Al ₂ O ₃)	<0.1%

For this contact, the amounts of Mg and Si were about the same as the bulk Al alloy so there did not seem to be any surface enrichment of Mg₂Si which was suspected as a source of the high resistance. When about 100Å of this surface was removed by ion etching, the N, S, F, and C were greatly reduced, which suggested that they may be a source of interfacial contamination.

The large percentage of carbon measured (31%) is believed to be a result of the photoresist leaving a carbon residue on the wafer. The composition of this photoresist could not be obtained from the manufacturer.

It should be noted that the composition of the structural grade Al 6061 consist of the following impurities:

Si	0.4 - 0.8%
Cu	0.15 - 0.4%
Fe	0.7%
Mg	0.8 - 1.2%
Mn	0.15%
Cr	0.15 - 0.35%
Zn	0.25%
Ti	0.15%

The primary reason for using this Al alloy was for the prevention of hillock formation.

Post heat treatment or sintering of a wafer exhibiting an initial poor yield (i.e. less than one kil-ohm for a chain of 560 vias in series) can increase the effective yield by 500 to 700% as

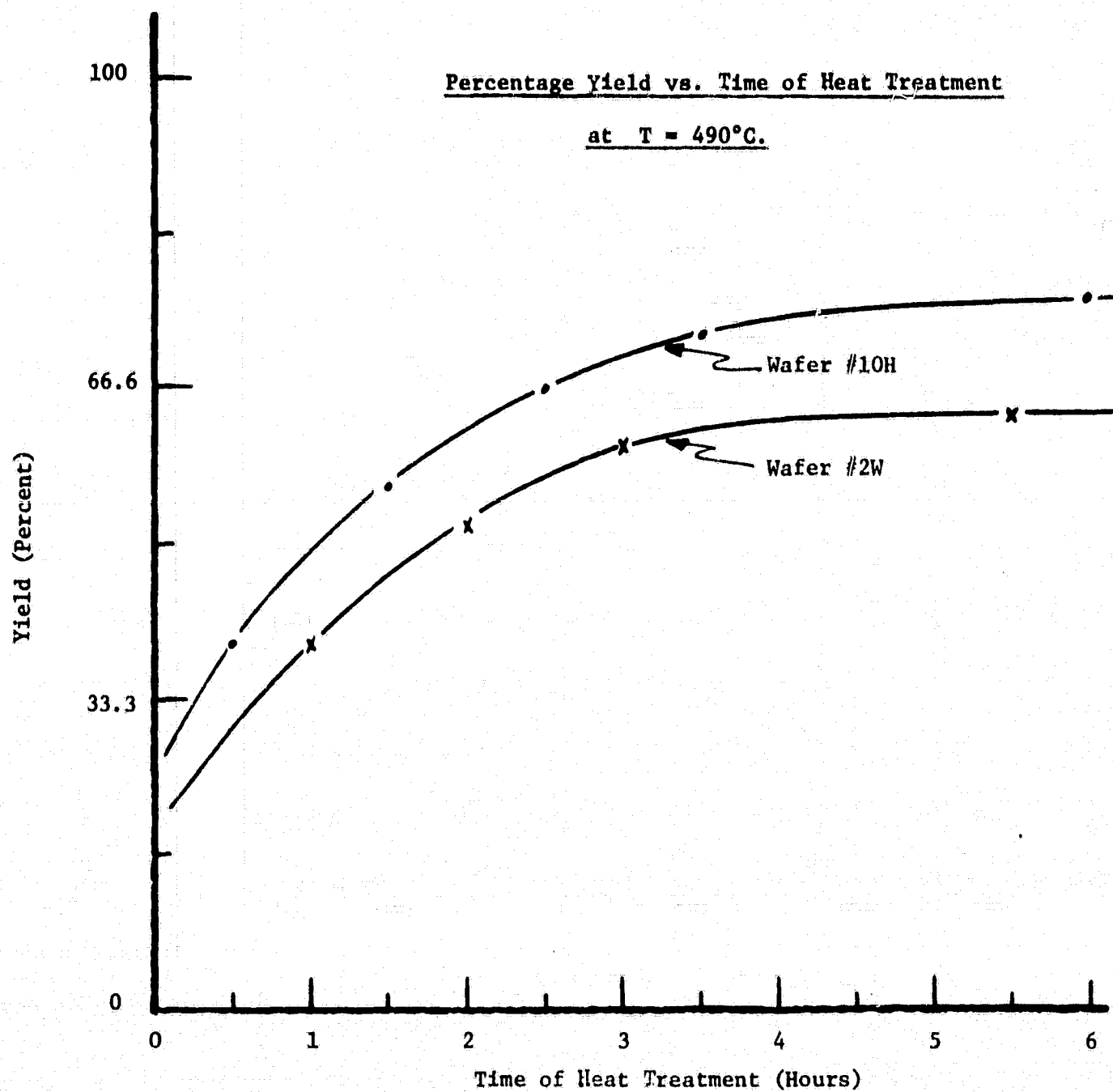


Figure F-3. Percentage yield of number of chips less than 1 kil ohm as a function time of heat treatment at 490°C for wafers with undoped intermetal dielectric.

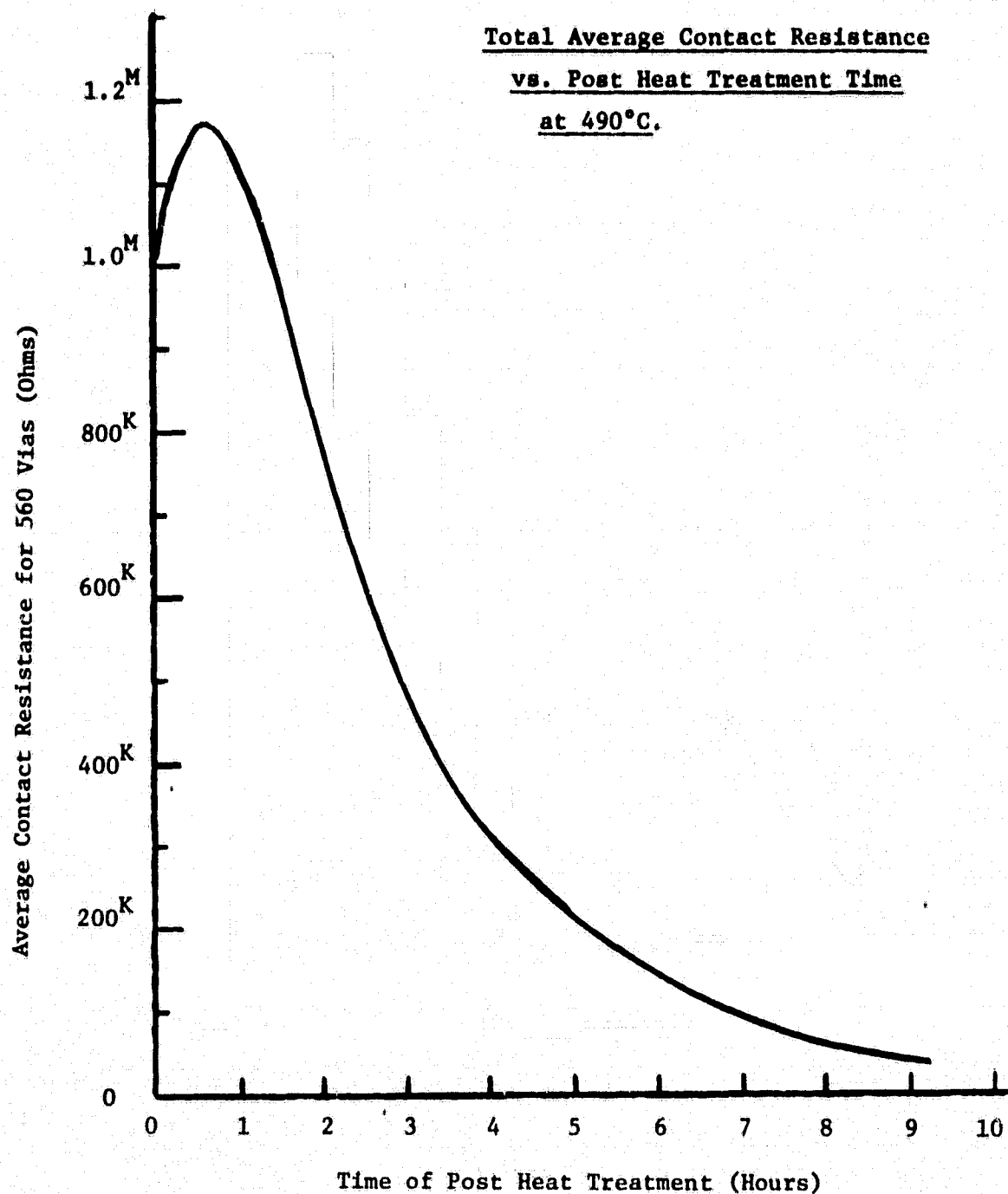


Figure F-4. Average contact resistance for 560 vias of all 0.5 mil square chips as a function of post heat treatment time for wafer #2W. (Total number of chips = 55)

illustrated in Figure 3 for wafers 10H and 2W. These wafers were processed as in 'C' above, having only a 15 minute 470°C sintering before initial testing. All addition sintering was done at 490°C in a nitrogen ambient.

The primary reason for this increase in yield with post heat treatment is due to the fact that the Al-to-Al contact resistance decreases with sintering, as demonstrated in Figure 4. Here, the average resistance for all test patterns having 0.5 mil square vias (approximately 55 of the total 212 chips) is plotted as a function of sintering time. As the time of sintering increases, the number of test patterns having a contact resistance < 1 kil-ohm increases, hence the yield increases.

On an individual chip basis, the contact resistance for 560 vias per chip behaved as shown in Figure F-5. For a given wafer which initially exhibits a relatively poor yield, the number of chips behaving in the manner shown for chips #10C and 10W was approximately 51%, those behaving like chip #10R was 27% and those like chip #10T was 10%. The remaining chips either exhibited low initial contact resistance (<300 ohms) or were open-circuited (>20 meg-ohms). Those chips initially exhibiting a low contact resistance generally had their resistance lowered with increasing heat treatment, however a few chips showed a gradual increase in resistance with increased heat treatment time as shown in Figure F-6. It is believed that this increase in resistance is due primarily to the consumption of Al by SiO_2 to lessen the Al thickness. Since at 490°C Al reacts chemically with SiO_2 to lessen the Al thickness.

Since at 490°C Al reacts chemically with SiO_2 to form Al_2O_3 and free Si, Al is consumed at a rate of 210Å/hr. [F-15]

The most predominant trend found in sintering of double level metal test patterns is demonstrated in Figure F-7. As inferred from this plot of contact resistance as a function of post-heat treatment for these two wafers, the average contact resistance decreases drastically for the first few hours of sintering. Because of this feature, the realization of multiple level metal LSI having a large number of vias (>2000) is a distinct possibility.

One major problem involved in post heat treatment of double layer metal structures is that the dielectric (C.V.D. - SiO_2) has a tendency to crack or "craze" at elevated temperatures (>500°C). This cracking, as illustrated in Figure F-8, is due to excess stress on the insulating layer [F.9]. One method to lessen, if not-alleviate this problem, is to use a phosphorous doped dielectric of 3 to 5 mole percent. This increases the effective temperature for which sintering can be done before cracking is observed [F.9].

Using this phosphorous doped dielectric (also called phosphosilicate glass or PSG) resulted in a much higher yield as shown in Table 1 and also a considerable less contact resistance as shown in Figure F-9. Here the average contact resistance as a function of via size is plotted for a test pattern with a doped dielectric layer for no heat treatment (curve B) and with 30 minutes post heat treatment at 490°C (curve A). These results are compared to the best results obtained for the undoped case (curve C),

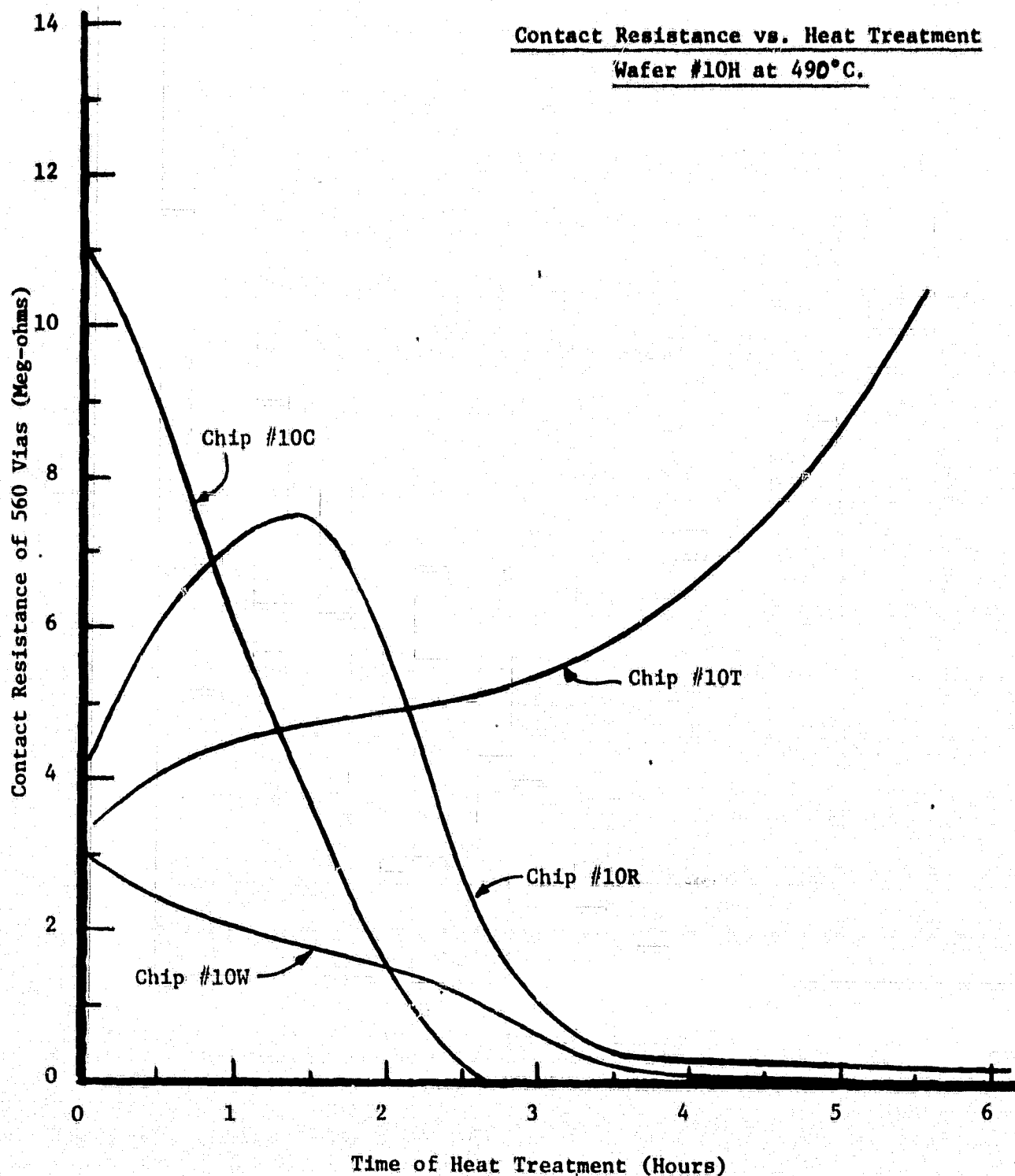


Figure F-5. Contact resistance of 560 vias as a function of heat treatment time for several different chips of wafer #10H at a temperature of 490°C.

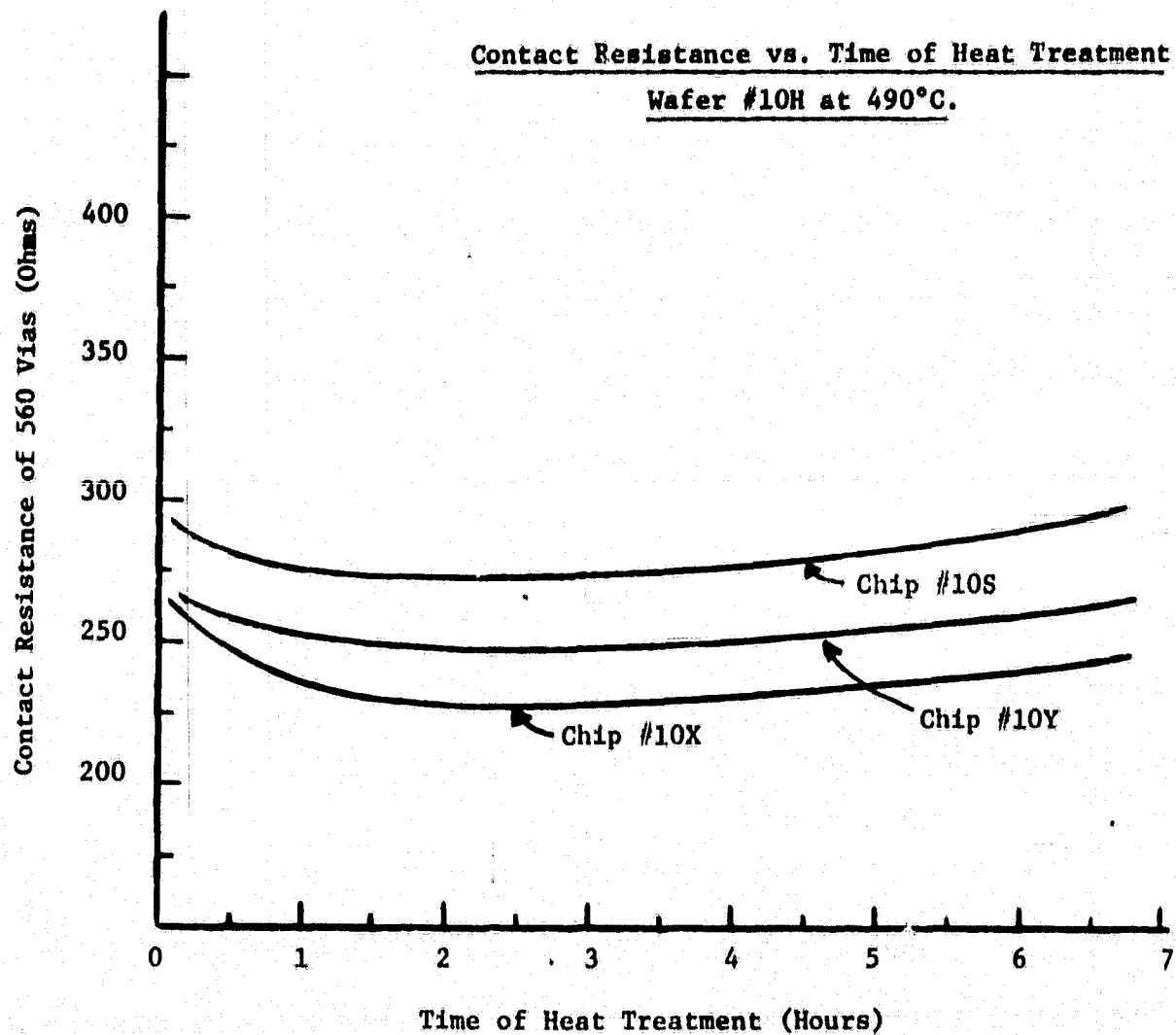


Figure F-6. Contact resistance of 560 vias as a function of heat treatment time for wafer #10H showing slight increase in resistance with time of heat treatment for "6% of the chips on the wafer.

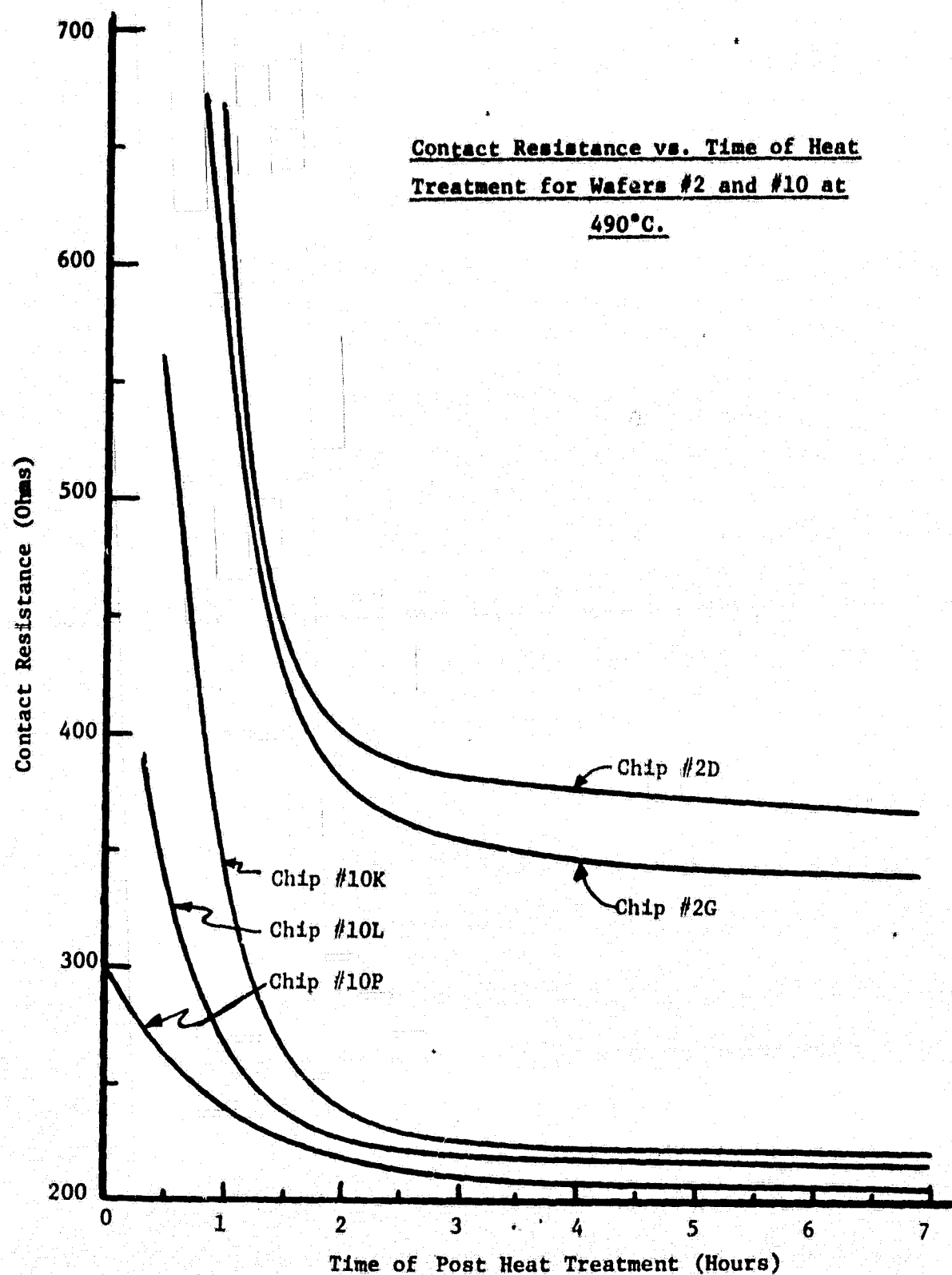


Figure F-7. Contact resistance trends as a function of heat treatment time for wafers #2 and #10.

even after many hours of heat treatment. The table in the figure indicates resistance and percent yield for each case presented.

A resistance map of the wafer shown in curve B is given below:

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173 159 154 217 161 143 158 196 176
170 171  ∞ 157 231 158 161 159 183 171 158
166 163 168 158 166 226 162 162 162 171 167 161 164
164 164 167 161 158 208 164 159 161 172 170 163 165 173
168 170 170 160 159 212 163 161 163 228 169 164  ∞ 172 164
157 168 169 170 165 158 219 162 161 160 234 168 163 163 170 160
164 170 170 171 164 156 213 161 163 159 221 173 159 163 170 165
112 173 201 176 164 151 143 173  ∞ 163 192 174 162 162 170 171
164 175 375 181 167 159 405 172 162 158 181 167 161 164 167 165
177 202 182 169 159 211 164 161 154 176 164 160 156 166
176 216 184 171 161 228 169 158 154  ∞ 162 156 154 165
44 198 179 171 162 228 164 158 153 173 160 157 151
260 181 171 163 231 166 159 154 172 160 153
177 166 200 167 159 151 167 157

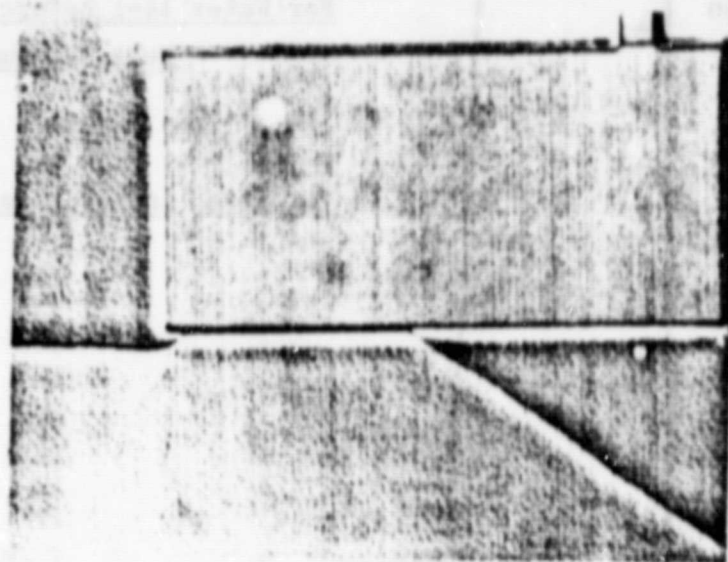
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Via size .4 .5 .2 .3 .4 .5 .2 .3 .4 .5 .2 .3 .4 .5 .2 .3 .4

D. Analysis and Conclusions

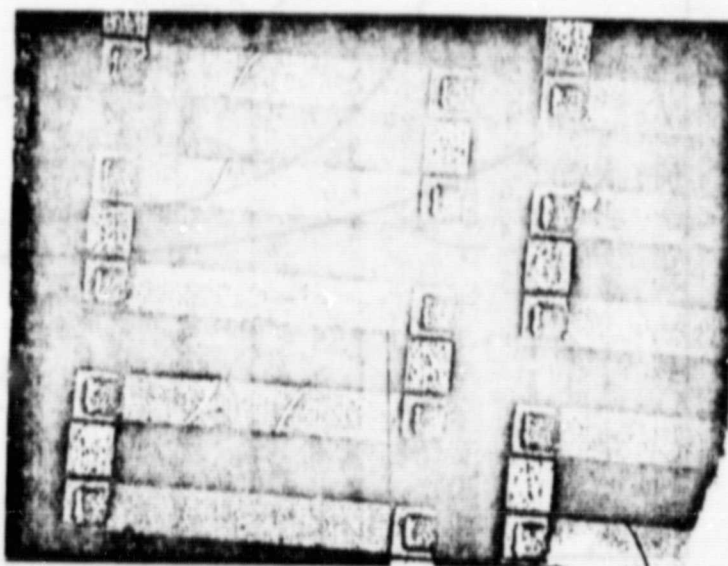
The following comments and conclusions may be derived from this investigation.

1) The variation in width of the metal interconnects between vias had little influence on yield, as expected. It may have had a slight effect on total resistance, especially for the 0.4 mil compared to 0.7 mil wide interconnect, but this was not detectable. The major difficulty came in mask alignment of the smaller interconnects.



Photomicrograph (A)

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Photomicrograph (B)

Figure F-8. Photomicrograph of test pattern at 300X magnification illustrating crazing tendency at temperatures $>500^{\circ}\text{C}$ and for fast pull from the furnace. Photomicrograph (A) shows crazing around a test pad whereas (B) shows crazing in the test pattern itself.

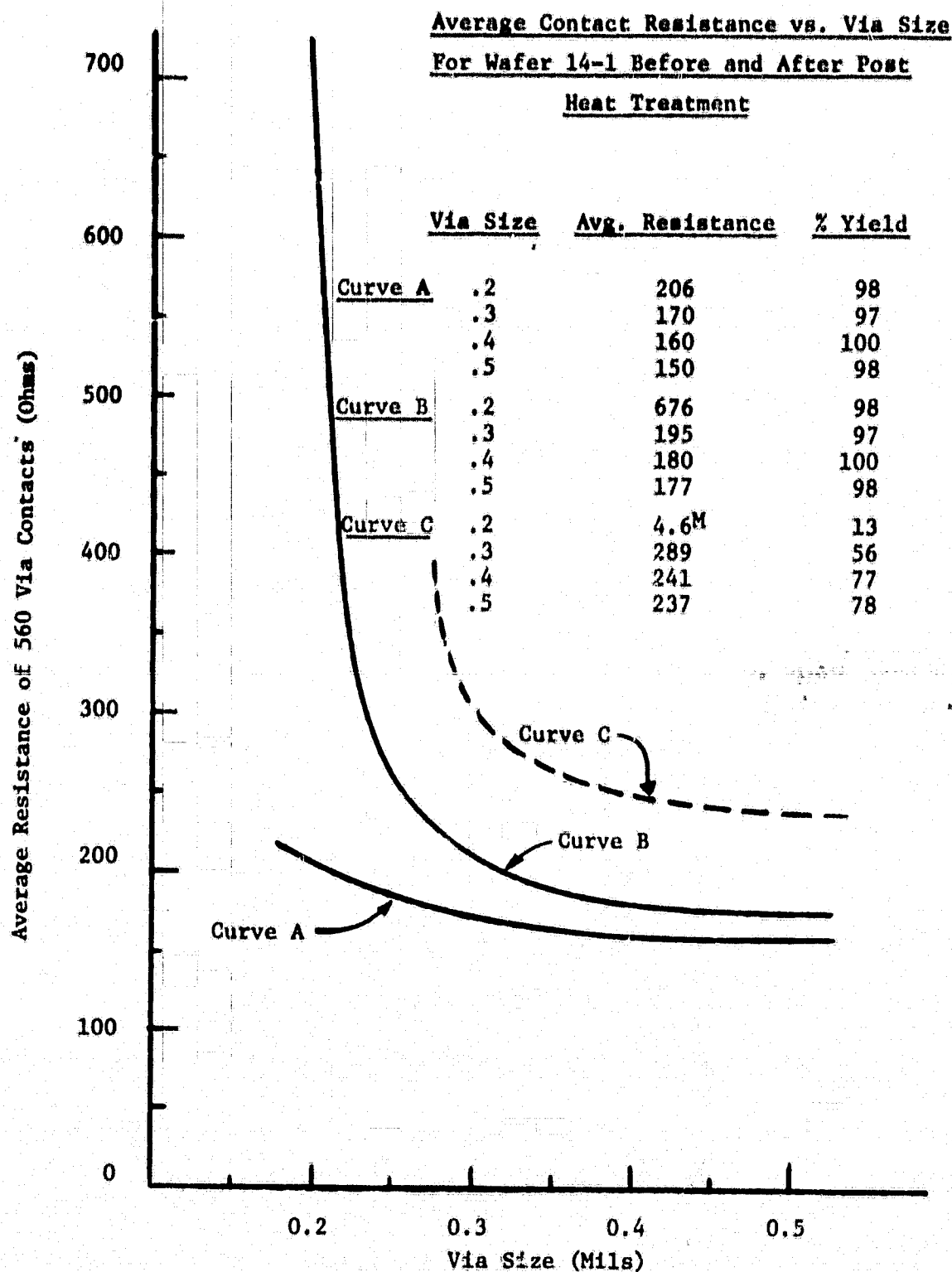


Figure F-9. Average contact resistance vs. via size for wafer #14-1 having phosphorous doped intermetal dielectric before post heat treatment (curve B) and after 30 minutes at 490°C (curve A). For comparison with a wafer having an undoped dielectric, curve C represents such a wafer after undergone 8 hours of post heat treatment at 490°C. (Note contact resistance for 0.5 mil via of wafer in curve C prior to post heat treatment was 90 kilohms.)

2) The extension of the via etch time of the dielectric film for both the dipped (stirred) etching and the ultrasonic etching indicated a substantial improvement in yield with only a slight undercutting for extended times below 90 seconds. (As expected, the doped dielectric etched faster than the undoped.) For etch times beyond break in excess of 110 seconds; the yield decreased. This is believed to be attributed to an increase in contact resistance- and thus a decrease in yield - due to a chemical reaction between the dielectric etchant and the alloys of the sputtered aluminum to form an insulating layer at the surface of the first level metal prior to depositing the second layer.

As indicated in Figure F-2, the optimum etch time is dependent on the size via being etched.

3) The addition of phosphorous doping to the oxide eliminated the possibility of intermetal dielectric cracking for post heat treatment temperatures below 500°C. A considerable increase in yield was also realized, having total average contact resistances slightly over 200 ohms for 0.5 mil vias and 250 ohms for 0.2 mil as per Figure F-9. (A slow pull of the wafer from the furnace was also practiced to eliminate cracking.)

4) The use of an ultrasonic etching bath for etching vias gives a much better probability of etching small vias (<0.2 mils). This etching was accomplished in a completely enclosed container.

5) The chemical cleaning of the first level metal through the vias prior to depositing the second level metal also increased yield. The first layer Al develops a thin oxide coating as soon as

it is exposed to the atmosphere and this oxide skin creates a high resistance upon depositing the second layer. This coupled with the difficulty of removing all of the dielectric film from the via and the formation of oxides of the alloys contained within the Al all tend toward low yield, high resistance contacts. There are actually two approaches for solving this problem, back sputtering and chemical etching. Back sputtering has the advantage that the oxide thickness can in principle be reduced to zero if the subsequent metallization is applied without exposure to air. The disadvantages include: possibility of radiation induced MOS damage; potential for contamination of the sputtering system; redeposition of previously sputtered materials especially from the substrate table; etc. The chemical etch procedure does not have these disadvantages, but the oxide thickness can never be reduced to zero. [F.14]

The use of a 1:1:1 ethylene glycol: buffered $\text{-HF} : \text{H}_2\text{O}$ etch removes all but 30-50 Å of oxide [F.10] without attacking the Al. (The second layer sputtered Al can easily penetrate this oxide thickness to form good ohmic contacts.) This etch was done just prior to second level metallization.

6) The application of post heat treatments can drastically increase yield by lowering total via contact resistance. There are several possible reactions which could occur to cause this temperature effect. [F.11] Aluminum could react with aluminum suboxides and thus break up the continuous layer of dielectric. Alternately, the recrystallization of aluminum in both of the

level could mechanically disrupt the thin native oxide layer, therefore forming aluminum-to-aluminum contact. As yet, there is no evidence for this speculation.

Figures F-4 and F-5 indicate that in some cases the contact resistance increases with post heat treatment time prior to the "diffusion" through this 'interfacial contamination' by the two layers of aluminum. If this contamination were SiO_2 , then it could be said that there exists excess ionic silicon in the oxide which becomes tied-up upon the application of post heat treatments [F-1]]. Since the contamination is probably Al_2O_3 , one might say there exist excess ionized Al in the oxide which reacts with the oxidizing species during the sintering process, thus decreasing the total ionic charge in the oxide layer causing the net resistance to increase.

7) Testing the via test pattern can be tedious. For high resistance vias the measured resistance was seen to be both light sensitive and current sensitive. As a result, all testing was accomplished in the dark. Ideally, very low testing potentials are applied in order not to break down a barrier layer thus turning a defective via into a good one. Also, theoretically, vias should not be tested in series, since the entire applied voltage will be dropped across a defective via, probably causing it to break down and appear good. However, in our testing, all vias were measured at once in series using a digital voltmeter.

8) Recently, a new planar multilevel interconnection technology was introduced [F.13] using polyimide films. Although

this procedure appears to be very promising for future applications if taken at face value, it is felt there is still many facets of "magic" associated with it.

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